VLSI Potentiostat Array With Oversampling Gain Modulation for Wide-Range Neurotransmitter Sensing

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Invited Paper

***Abstract*—A 16-channel current-measuring very large-scale integration (VLSI) sensor array system for highly sensitive electrochemical detection of electroactive neurotransmiters like dopamine and nitric-oxide is presented. Each channel embeds a current integrating potentiostat within a switched-capacitor first-order single-bit delta–sigma modulator implementing an incremental analog-to-digital converter. The duty-cycle modulation of current feedback in the delta–sigma loop together with variable oversampling ratio provide a programmable digital range selection of the input current spanning over six orders of magnitude from picoamperes to microamperes. The array offers 100-fA input current sensitivity at 3.4-μW power consumption per channel. The operation of the 3 mm $\times$ 3 mm chip fabricated in 0.5-μm CMOS technology is demonstrated with real-time multichannel acquisition of neurotransmitter concentration.**

***Index Terms*—Biomedical instrumentation, correlated double sampling, current measurement, micropower techniques, potentiostat, sigma–delta modulator, switched-capacitor circuits.**

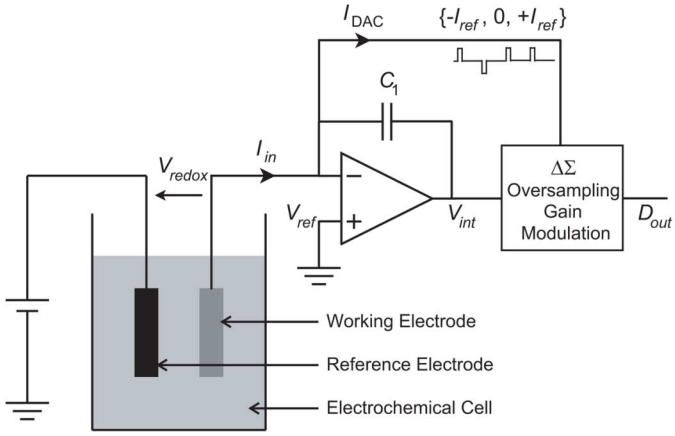

Fig. 1. Simplified schematic of potentiostat system and interfacing electrochemical cell.

I. Introduction

STUDIES of neural pathways and the etiology of neurological diseases, like epilepsy and stroke, require real-time and sensitive detection and monitoring of neurotransmitters. Neurotransmitters are molecular messengers across the electrically insulating synaptic gaps between neurons. Electrochemical detection is the preferred means of neurotransmitter measurement due to its high sensitivity, its fast detection speed, and its ability to perform distributed measurements [1]–[3].

Electrochemical analysis requires measuring the current generated by a chemical reaction, involving the species of interest, at an electrode held at a characteristic potential, the redox potential for that species [4]. The concentration of the species is transduced at the *working* electrode which is held at the redox potential with respect to the *reference* electrode as shown in Fig. 1. The instrument used to measure current at the redox potential is a potentiostat. Currently electrochemical analysis of neurotransmitters requires a benchtop potentiostat. Analysis is limited by the size, sensitivity and cost of the instrument. The ability to record neurotransmitter levels from a population of neurons, rather than a single cell, is of tremendous potential. Sensor arrays can be microfabricated to perform high spatial resolution sensing. Integrated multichannel potentiostats interfacing with sensor arrays allow joint recording of several signals of interest. VLSI technology offers several advantages for implementation of a highly integrated potentiostat array: high sensitivity, small feature size, low noise, low power and modularity.

In previous VLSI designs of integrated potentiostats with one or few parallel channels, small input currents in the picoampere to nanoampere range were amplified to microampere range to facilitate current-mode analog-to-digital conversion [5]–[11]. By directly integrating the current input within a current feedback modulator loop [12]–[14], we avoid the imprecision introduced by the amplification stage. The integration of the input current is embedded within a single-bit

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delta–sigma modulator loop implementing a first-order incremental analog-to-digital converter for increased sensitivity and integrated digital output [15]. Range selection over six decades of input current is performed by a combination of variable duty cycle of current feedback and variable oversampling ratio in the delta–sigma modulator.

Low-power implementation of the potentiostat array makes it amenable to implantation where the power source is a microbattery or passive RF telemetry based on inductive coupling. A VLSI design capable of powering both chips under normal operating conditions has been developed [16]. The sensor probes can be fabricated on the same substrate as the potentiostat and telemetry circuitry, creating a fully integrated stand-alone implanted wireless probe capable of transducing, sensing, processing and transmitting neurotransmitter signals [17].

The principle of digital gain modulation, and system level description of the potentiostat with biomedical applications are described in a companion paper [15]. Here we present details on the VLSI circuit implementation, analysis of precision and noise performance, and further characterization of the circuits on multichannel neurotransmitter measurements. The architecture and circuit-level implementation of the potentiostat with delta–sigma modulator and decimator are presented in Section II. Section III analyzes the design and quantifies the performance of the implemented circuits. Experimental characterization of a fabricated prototype and real-time neurotransmitter measurements using electrode array are presented in Section IV, followed by the concluding comments in Section V.

II. Chip Architecture

The input current ranges from picoamperes to microamperes, with time scales ranging from milliseconds to seconds. This wide range of currents calls for multiple scales of measurement, while the long time constants allow for long integration times. Long integration times call for oversampling and support the use of a lower order delta–sigma modulator. Delta–sigma oversampled data conversion avoids the need for low-pass anti-alias filtering in the input, and decimation reduces high-frequency noise present in the current signal along with the shaped quantization noise.

Wide dynamic range over multiple scales of input current is achieved by a gain-modulation scheme implemented as a variable duty cycle shunting sequence in the digital-to-analog (D/A) feedback loop of the delta–sigma modulator. Digital control over the duty cycle of the shunting sequence directly sets the gain of input amplification, since the duty cycle effectively shunts the strength of the reference signal in the D/A feedback loop by the same factor. Digital shunting of the reference signal is more precise than analog scaling of the reference current, which is prone to mismatch errors. A precise gain factor G is achieved by passing the D/A feedback for a single clock cycle followed by $G-1$ clock cycles of shunting the feedback. Even though the digital gain modulation over G clock cycles reduces the conversion rate by a factor G, it produces more precise results than increasing the delta–sigma oversampling ratio (OSR) by the same factor owing to reduced noise, as we analyze in Section III and experimentally validate in Section IV. With fixed reference current but variable feedback digital gain

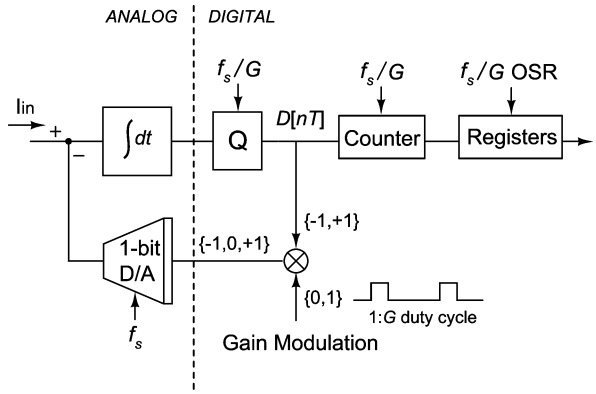

Fig. 2. System level diagram of a single channel of the potentiostat.

G and also variable oversampling ratio OSR, the potentiostat is capable of ranging digitally over a wide range of currents, spanning six decades from 100 fA to 500 nA.

The digitizing potentiostat is implemented as a first-order incremental analog-to-digital converter (ADC), a version of the first-order delta–sigma modulator with a counting decimator [18]. A block diagram for one channel of the potentiostat array is shown in Fig. 2. The first-order incremental topology is amenable to simple and compact implementation, leading to significant savings in silicon area and power consumption. A sampled-data switched-capacitor (SC) realization offers low-noise and low-power implementation. Single-bit quantization leads to very robust circuits, relaxing linearity constraints in the design of the D/A converter with decreased sensitivity to mismatch errors. Gain modulation is implemented by shunting the D/A feedback, turning the binary $\{-1,+1\}$ feedback signal into a trinary $\{-1,0,+1\}$ level signal.

The decimator is implemented using a binary counter, which is clocked synchronous with the rate of digital gain modulation, f_S/G. The decimated digital value is buffered in a register at the end of the conversion cycle, at a rate $f_S/G\mathrm{OSR}$. The digital outputs from all 16 channels are read out asynchronously in bit serial form using an output shift register.

A. Delta–Sigma Modulator

The first-order delta–sigma modulator comprises a current integrator, comparator, and switched-current single-bit D/A converter (DAC) with variable digital gain duty-cycle modulation. The integrator and switched-current DAC are shown in Fig. 3.

1) Current Integrator: To achieve high resolution and minimize distortion, the input current is directly integrated onto a capacitor C_1 in the feedback loop of a low-noise high-gain sense amplifier, converting the integrated current into a voltage signal. One of two values of the current integrating capacitance C_1, 100 fF, or 1.1 pF, is selected by the *scale* bit. The choice of integrating capacitance C_1 depends on the input current range and implies a tradeoff between conversion speed and noise performance as analyzed in Section III.

Instead of using a differential operational amplifier as high gain element in the current integrator, we have chosen to use a lower power, single ended inverting amplifier. Correlated double sampling (CDS) establishes the voltage at the virtual

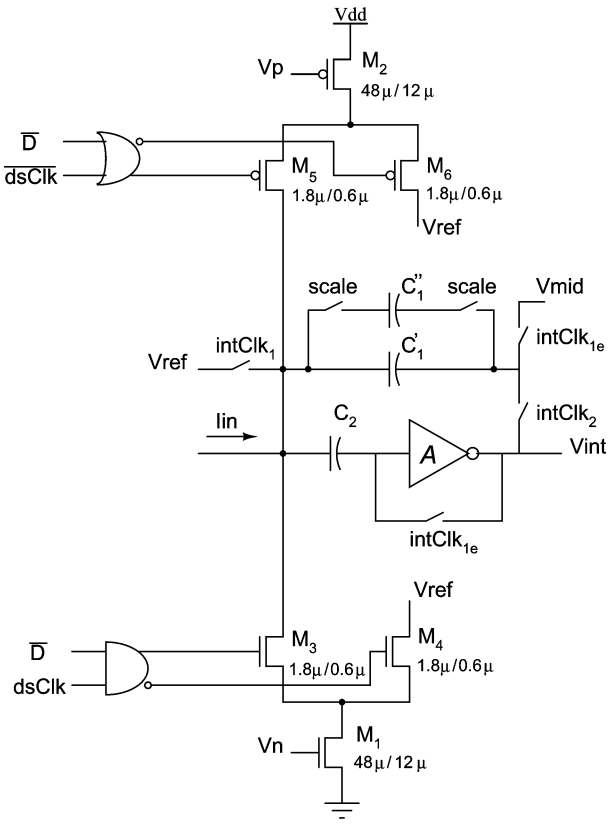

Fig. 3. Schematic of delta–sigma current integrator with switched-current single-bit DAC.

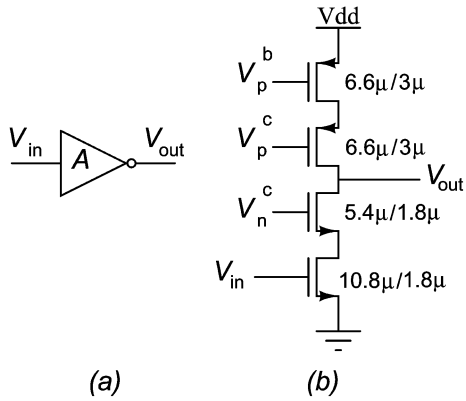

Fig. 4. Cascoded inverter as high-gain amplifier. (a) Circuit symbol. (b) Circuit implementation.

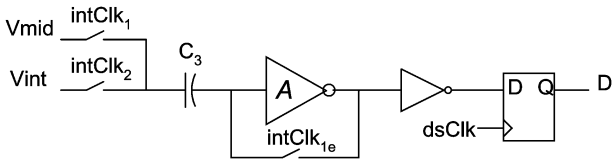

Fig. 5. Circuit schematic of comparator used as single-bit quantizer in the delta–sigma modulator.

ground input to the integrator through a coupling capacitor C_2 inserted in between the integrator input and the inverting amplifier. The capacitor C_2 samples the difference between the inverting amplifier offset and the externally supplied voltage reference $V_{\rm ref}$ at the beginning of the conversion cycle, activated by the *intClk* clock signal. The capacitance C_2 is 1 pF to minimize the effect of charge leakage over the length of the conversion cycle.

The design of the single-stage cascoded inverting amplifier in the current integrator is shown in Fig. 4. The choice of telescopic operational amplifier without tail transistor results in high density of integration and reduced noise and power dissipation [19], and the CDS across the amplifier further reduces effects of flicker $(1/f)$ noise [20]. For highest energy efficiency the amplifier is biased on the verge of the subthreshold regime, where the amplifier has maximum transconductance-to-current ratio and low power consumption. The subthreshold operation also provides extended output dynamic range with minimum drain-to-source saturation voltage. The bias current of the amplifier is set by the voltage bias $V_p{}^b$ to the minimum value that accommodates adequate slew rate relative to the sampling frequency. At 200 nA of biasing current, 1 pF load capacitance and 3 V supply, simulations indicate an open-loop dc gain of 91 dB and gain–bandwidth product of 844.3 kHz. No additional gain-boosting techniques were attempted, since the dc gain provided was sufficient for the target resolution.

2) Current Feedback DAC: Single-bit D/A conversion and duty-cycle modulation in the delta–sigma feedback loop are implemented by a switched current circuit comprising transistors M_1–M_6. The switched currents feed directly into the input node, where they are integrated along with the input current. The current sourcing transistors $M1$ and $M2$ generating tail currents $\pm I_{\rm ref}$ are sized with large width and length ($W = 48\ \mu$m, $L = 12\ \mu$m) to improve matching between reference currents across channels. Bias voltages V_p and V_n are set with a single externally supplied current reference $I_{\rm ref}$. Transistors M_3, M_4, M_5, and M_6 implement minimum-size switches to direct the reference current either into the integrator or to a shunting path at the same reference voltage level $V_{\rm ref}$. Therefore, the current sources M_1 and M_2 are always active, and their drain voltage is maintained at the reference voltage level $V_{\rm ref}$, decreasing the effect of charge injection noise at the integrator input.

Shunting of the feedback current is controlled by the digital gain modulation clock *dsClk*. When *dsClk* is active, one polarity of reference current is injected into the integrating node depending on the quantization bit D from the comparator. When *dsClk* is low, both currents are diverted to the shunting path and cancel onto the $V_{\rm ref}$ node.

3) Comparator: Single-bit quantization in the delta–sigma modulator is implemented by the comparator shown in Fig. 5. The comparator is reset at the beginning of each integration cycle when clock $intClk_1$ is active and coupling capacitor C_3 (1 pF) samples the mid level voltage $V_{\rm mid}$. In the conversion phase, when clock $intClk_1$ is low, the difference between the integrator output voltage $V_{\rm int}$ and $V_{\rm mid}$ is amplified, and the result of comparison is latched on the falling edge of clock *dsClk*. The same single-stage cascoded inverting amplifier of Fig. 4 is used as high-gain amplifier in the comparator.

4) Clock Timing: The timing of all clocks is generated from a system clock *sysClk* at sampling rate f_s, nominally 2 MHz. Digital gain modulation is served by clock *dsClk*, active for a single

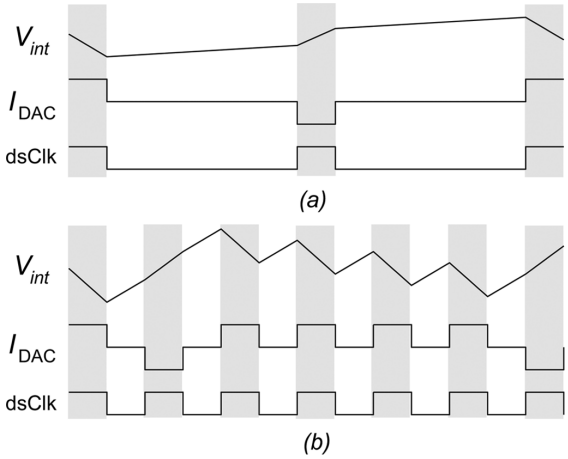

Fig. 6. Effect of duty cycle modulation of delta–sigma feedback on the integrated current, illustrated for two values of digital gain G. (a) Lower scale of currents at $G = 6$. (b) Higher scale of currents at $G = 2$.

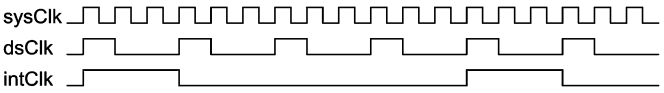

Fig. 7. Gain modulation clock *dsClk* and integration clock *intClk*, illustrated for digital gain $G = 3$ and oversampling ratio $\mathrm{OSR} = 4$.

cycle in every G cycles, at a rate f_s/G. Example waveforms of the integrator output for different values of G are shown in Fig. 6. The digital gain modulation clock *dsClk* also clocks the counter in the decimator. The decimated output is available after OSR cycles of $dsClk$, at a conversion rate $f_s/G\mathrm{OSR}$ controlled by integrator clock *intClk*. Active during the first $dsClk$ cycle, *intClk* buffers the decimated output and resets the integrator, comparator and counter for the next conversion cycle. Example clock signals *dsClk* and *intClk* generated from *sysClk* are illustrated in Fig. 7; typical values of G and OSR are much larger in practice (between 1 and 2^{16}).

From the integrator clock *intClk* nonoverlapping clocks $intClk_1$ and $intClk_2$ are derived. The clock $intClk_{1e}$ is the replica of clock $intClk_1$ with rising edge following the rising edge of $intClk_1$ and falling edge preceding the falling edge of the clock $intClk_1$. All the switches are implemented with complementary transmission gate MOSFETs, except the switches controlled by $intClk_{1e}$, implemented as n-channel MOSFETs.

The operation of the modulator over one conversion cycle is summarized as follows. In the reset phase, at the beginning of the conversion cycle, $intClk_1$ is active which precharges C_1 in Fig. 3 to set the integrator input to reference voltage V_{ref} and set the integrator output to the mid point of the voltage range, V_{mid}. On the rising edge of $intClk_{1e}$ the inverting amplifier resets, charging C_2 to sample the difference between V_{ref} and the inverting amplifier threshold. The precharging operations are completed on the falling edge of $intClk_{1e}$, the external reference V_{ref} is disconnected on the falling edge of $intClk_1$, and the integration across C_1 starts on the rising edge of $intClk_2$. The sequence of clocks $intClk_1$, $intClk_{1e}$ and $intClk_2$ implements a CDS operation which removes the offset of the amplifier and establishes a virtual ground at level V_{ref} at the input of the integrator. In similar fashion, and synchronous with integrator reset, the *intClk* sequence controls reset of the comparator in Fig. 5 by precharging C_3 to remove the offset of the amplifier and set the threshold of the comparator to voltage level V_{mid}.

The input current is continuously integrated on capacitor C_1, while the feedback current from the D/A converter is integrated only when the clock *dsClk* is high, at a variable duty cycle set by digital gain G. The single-bit quantization result D from the comparator is latched on rising edge of clock *dsClk*.

B. Decimator and Serial Output

The decimator is implemented as the simple accumulate-and-dump circuit. The output bits of delta–sigma modulator that represent logic one are counted using 16-bit counter during one conversion period. The conversion period is programmable and represents the period of clock *intClk*. At the end of each conversion cycle, the counter value is written to output register and a new conversion cycle begins with cleared counter. The register can be read asynchronously at any time during conversion cycle. The 16 bits representing the digital value of input current of each channel are shifted out bit-serially using clock independent of system clock and 256 cycles are necessary to read out all 16 channels. The output serial bitstream is amenable to downlink telemetry in an implantable device for transcutaneous communication.

III. Performance Limitations and Noise

1) Range and Resolution: The incremental delta–sigma converter resets the integrator at the beginning of each conversion period. At time nT from reset, with $T = G/f_s$ the period of clock *dsClk*, the integrator output voltage V_{int} equals

$$V_{\mathrm{int}}[n+1] = V_{\mathrm{int}}[n] + \left(I_{\mathrm{in}} - D[n]\frac{I_{\mathrm{ref}}}{G}\right)\frac{T}{C_1} \qquad (1)$$

where $D[n]$ is the comparator output (-1 or $+1$) at time nT, with initial conditions $V_{\mathrm{int}}[0] = V_{\mathrm{mid}} = 0$ and $D[0] = -1$. At the end of the conversion period, after a number of integration cycles equal to the oversampling ratio OSR, the integrator voltage reaches its final value

$$V_{\mathrm{int}}[\mathrm{OSR}] = \left(\mathrm{OSR}\ I_{\mathrm{in}} - \sum_{i=1}^{\mathrm{OSR}-1} D[i]\frac{I_{\mathrm{ref}}}{G}\right)\frac{T}{C_1}. \qquad (2)$$

Therefore, the input current I_{in} (or its average over the integration interval) decomposes into two terms as

$$I_{\mathrm{in}} = \sum_{i=1}^{\mathrm{OSR}-1} D[i]\frac{I_{\mathrm{ref}}}{G\,\mathrm{OSR}} + \frac{V_{\mathrm{int}}[\mathrm{OSR}]}{\mathrm{OSR}}\frac{C_1}{T} \qquad (3)$$

where the first term represents the decimated output, and the second term represents the conversion error. The decimated output term defines the least significant bit (LSB) resolution of the input current as

$$I_{\mathrm{lsb}} = \frac{2I_{\mathrm{ref}}}{G\,\mathrm{OSR}}. \qquad (4)$$

The resolution is thus given by the reference current I_{ref} scaled by both the digital gain G and the oversampling ratio OSR, whereas the range of input current $2I_{\mathrm{ref}}/G$ is scaled by the

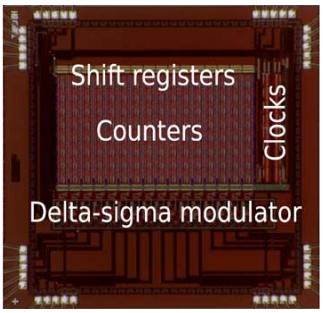

Fig. 8. Micrograph of the 16-channel potentiostat. Die size is 3×3 mm^2 in 0.5-μm CMOS technology.

digital gain G only. Correspondingly, the conversion rate $f_{\rm conv}$ equals

$$f_{\rm conv} = \frac{f_s}{G\,\mathrm{OSR}} \tag{5}$$

which implies a linear tradeoff between resolution and conversion bandwidth. This tradeoff is further quantified in terms of the voltage range of the integrator.

From (3) the range of the integrator output voltage $V_{\rm int}$, covering an LSB change in the quantized output, equals

$$V_{\rm range} = 2\frac{I_{\rm ref}}{G}\frac{T}{C_1} = 2\frac{I_{\rm ref}}{f_s C_1} \tag{6}$$

which corresponds to the voltage excursion across the integrator with the reference current $I_{\rm ref}$ active over one master clock cycle $1/f_s$. By combining (4)–(6), we obtain a more fundamental relation between resolution and bandwidth

$$I_{\rm lsb} = f_{\rm conv}\, C_1 V_{\rm range} \tag{7}$$

which reflects that the voltage excursion corresponding to an LSB increment in the input current over one conversion cycle covers the range of the integrator. From (7) the resolution $I_{\rm lsb}$ that can be attained for a given bandwidth $f_{\rm conv}$ depends only on the value of the integrating capacitor C_1. For a capacitance of 1.1 pF, the input current can be resolved with 100 fA sensitivity in 10 s, as is shown in Section IV, Fig. 9. For the smaller value of the integrating capacitance $C_1 = 0.1$ pF, the conversion time is reduced to 1 s at the expense of increased thermal noise in the input voltage. For stability the capacitance C_1 should be larger than the parasitic capacitance at the potentiostat input divided by the gain of the inverting amplifier, which decreases with increasing frequency of fluctuations coupling into the input. The factor G reduction in the bandwidth of current feedback by gain modulation thus also contributes to the stability of the input voltage.

From (7), the current sensitivity appears to be independent of the digital gain G introduced through modulation of current feedback. The obtained resolution for a given conversion bandwidth and sampling rate depends only on the product of G and OSR, and would in principle be identical for an incremental data converter without gain modulation ($G = 0$) and with oversampling ratio G OSR. However, the introduction of digital gain modulation reduces the activity of current feedback onto the input and digital switching in the decimator, and thus reduces noise and power consumption at the same nominal sensitivity and conversion rate. To obtain the same nominal resolution $I_{\rm lsb}$, the incremental data converter without gain modulation requires G OSR cycles of pulsed current integration, a factor G larger than the gain modulated converter. The effect of gain modulated noise on current sensitivity is analyzed next.

2) Noise Analysis: The main sources of circuit noise affecting the performance of the potentiostat and current data con-

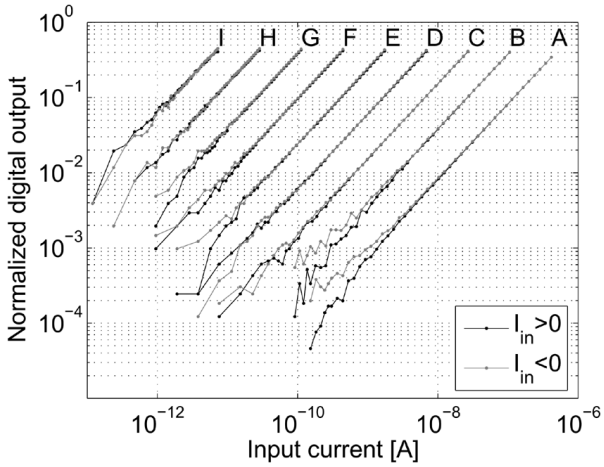

Fig. 9. Normalized digital output of the chip for several values of digital gain G, oversampling ratio OSR and both polarities of input currents [15].

TABLE I
PARAMETERS FOR CHARACTERIZATION TRACES SHOWN IN FIG. 9

Trace	*Gain* (G)	*OSR*	*Input current range*	*Conversion time* (ms)	*Power* mW
A	2^0	2^{16}	±500nA	32	1.27
B	2^2	2^{15}	±125nA	65	0.97
C	2^4	2^{14}	±30nA	131	0.67
D	2^6	2^{13}	±8nA	262	0.57
E	2^8	2^{12}	±2nA	524	0.54
F	2^{10}	2^{11}	±500pA	1048	0.54
G	2^{12}	2^{10}	±125pA	2097	0.54
H	2^{14}	2^9	±30pA	4194	0.54
I	2^{16}	2^8	±8pA	8388	0.54

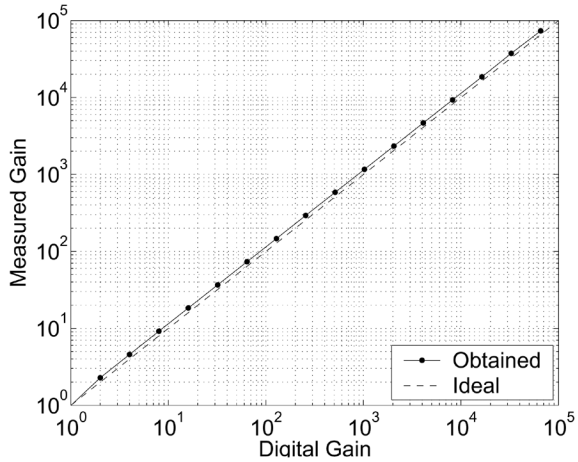

Fig. 10. Actual gain as a function of digitally programmed gain G of current measurement.

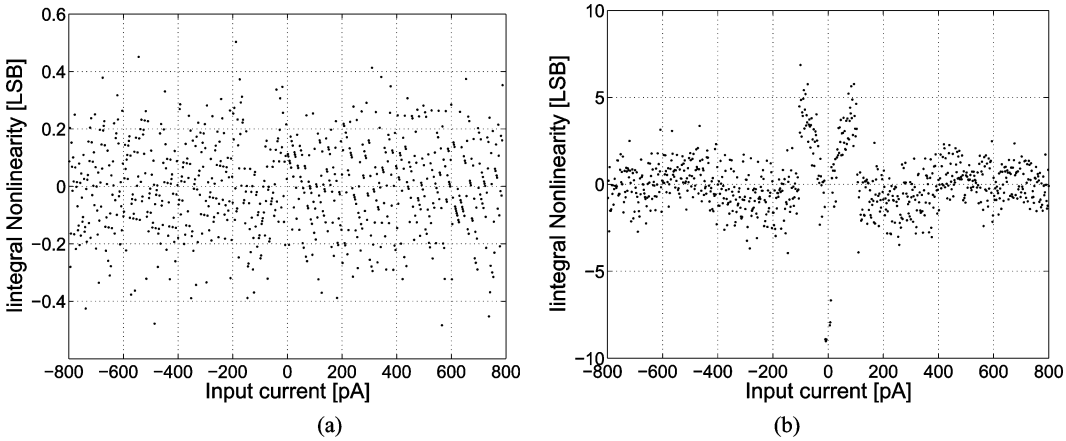

Fig. 11. Measured integral nonlinearity (INL) for (a) digital gain $G = 256$ and oversampling $\mathrm{OSR} = 256$ and (b) $G = 1$ and $\mathrm{OSR} = 2^{16}$ evaluated over the same range.

verter are the inverting amplifier in the integrator, and the DAC reference current sources.

The potentiostat voltage noise is determined by the input-referred voltage noise of the inverting amplifier, dominated by thermal noise of the input transistor operated in subthreshold. This noise contribution is shot noise limited with an input-referred spectral density [22]

$$v_{\mathrm{amp},n}^2 = 2{V_{\mathrm{th}}}^2 \frac{q}{\kappa^2 I_b} \Delta f \tag{8}$$

where $V_{\mathrm{th}} = kT_{\mathrm{abs}}/q$ is the thermal voltage, k is the Boltzmann constant, T_{abs} is absolute temperature, q is the elementary charge of the electron, κ is the gate effectiveness over bulk back-gate coupling, and I_b is the bias current of the amplifier. The contribution of flicker $(1/f)$ noise, the dominating noise source at low frequencies, is reduced owing to the effect of CDS [23] across the input capacitor C_2, at the conversion rate f_{conv}. The switch injection noise sampled on capacitor C_2 represents a dc offset to the electrode voltage which is minimized by relatively large sizing of C_2 (1 pF).

The input-referred current noise of the potentiostat and data converter is obtained by evaluating the effect of DAC current noise and integrator noise on the decimated output. According to (3), the effect of integrator noise in the decimated output is negligible since it amounts to a variation much smaller than an LSB. Noise in the reference current I_{ref} however directly impacts the decimated output since it is integrated along with the input current on C_1. The reference current noise density is given mainly by thermal noise in the DAC current sources $M1$ and $M2$

$$i_{\mathrm{ref},n}^2 = \frac{2}{3} 4kT_{\mathrm{abs}} g_{m1} \Delta f \tag{9}$$

where g_{m1} is the transconductance of the current sourcing transistor $M1$ operating above threshold. Other sources of noise acting on the DAC feedback current are flicker $(1/f)$ and switch injection noise. The effect of $1/f$ noise contributed by M_1 and M_2 is minimized by large transistor sizing ($W = 48\ \mu$m, $L = 12\ \mu$m). Noise contributions by charge injection in transistors M_3 and M_5 to the integrated reference current are mimimized by the differential switching topology in Fig. 3 that maintains a constant V_{ref} potential on the drains of $M1$ and $M2$.

Each gain modulation current feedback cycle contributes the noise density (9) over approximately f_s bandwidth, resulting in a total input-referred noise power

$$\begin{aligned} i_{\mathrm{in},n}^2 &\approx \sum_{i=1}^{\mathrm{OSR}-1} \frac{i_{\mathrm{ref},n}^2}{G^2 \mathrm{OSR}^2} \\ &\approx \frac{1}{G^2 \mathrm{OSR}} \frac{2}{3} 4kT_{\mathrm{abs}} g_{m1} f_s \\ &= \frac{8}{3} kT_{\mathrm{abs}} g_{m1} \frac{f_{\mathrm{conv}}}{G}. \end{aligned} \tag{10}$$

The advantage of gain modulation $G > 1$ in improving the current sensitivity of the potentiostat is evident. G-fold gain modulation at G-fold increased reference current yields $\sqrt{G}$-fold reduction in input-referred noise power because of the weak square-root dependence of transconductance on current in $M1$ $(M2)$ above threshold, $g_{m1} \propto \sqrt{I_{\mathrm{ref}}}$. However, at given nominal target resolution I_{lsb}(4) and given conversion bandwidth (7), the reference current I_{ref} is fixed, and gain modulation yields a net G-fold reduction in input-referred noise power, and hence an $\sqrt{G}$-fold improvement in current sensitivity of the potentiostat (compare with Fig. 11 for experimental validation). Gain modulation also affords a G-fold reduction in dynamic digital power dissipation in the counting decimator owing to the resulting G-fold reduction in oversampling ratio OSR.

3) Power Dissipation: Power dissipation is a limiting factor in the performance of the integrated potentiostat, especially for implantable applications with very low power budgets in the microwatt range. The power dissipation for one channel of the integrated potentiostat and data converter is approximated by

$$P_{\mathrm{diss}} = 2I_{\mathrm{ref}} V_{\mathrm{dd}} + 2I_b V_{\mathrm{dd}} + \frac{1}{G} f_{\mathrm{conv}} C_{\mathrm{dec}} V_{\mathrm{dd}}^2 \tag{11}$$

where the first term accounts for both DAC sources $M1$ and $M2$, the second term corresponds to the integrator and comparator amplifiers, and the last term the dynamic power of the decimator with equivalent internal capacitive load C_{dec}.

TABLE II
COMPARISON BETWEEN VLSI POTENTIOSTAT CHIPS

	Sensitivity	*Dynamic range*	*Channels*	*Power per channel*
Kakerow [6]	100pA	75dB	1	NA
Turner [5]	100nA	32dB	1	2mW
Breten [8]	$>$ 10pA	74dB	1	NA
Bandyopadhyay [9]	500pA	120dB	8	62.5μW
Narula [12]	1pA	116dB	1	0.13mW
Gore [13]	50fA	60dB	42	11μW
This work	100fA	140dB	16	3.4μW (G $> 2^8$)

The limit of energy efficiency for a given resolution G OSR can be readily estimated from (11). According to (4) and (7), the first term reduces to $G\,\mathrm{OSR}C_1 f_{\mathrm{conv}} V_{\mathrm{range}} V_{\mathrm{dd}}$. The biasing of the inverting amplifiers in the second term can be minimized subject to bandwidth requirements. To accomodate a signal swing V_{range} in the integrator over a fraction $\lambda < 1$ of one integration cycle $T = G/f_s$

$$I_b = \frac{1}{\lambda G} f_s C_1 V_{\mathrm{range}} \tag{12}$$

with an equivalent condition for the comparator biasing. The resulting power decomposes into analog and digital contributions

$$P_{\mathrm{diss}} = G\,\mathrm{OSR} f_{\mathrm{conv}} \left(\frac{2}{\lambda G} + 1\right) C_1 V_{\mathrm{range}} V_{\mathrm{dd}} + \frac{1}{G} f_{\mathrm{conv}} C_{\mathrm{dec}} V_{\mathrm{dd}}^2. \tag{13}$$

Gain modulation thus reduces the digital power, at the expense of analog power. Even so, for large G the analog power shows a linear dependence on resolution G OSR and bandwidth f_{conv}, tending to a constant figure of merit (FOM). The reciprocal of the FOM, defined as the energy consumed per conversion and per quantization level, is in the limit of large G

$$\frac{1}{\mathrm{FOM}} = C_1 V_{\mathrm{range}} V_{\mathrm{dd}}. \tag{14}$$

For $C_1 = C_3 = 1$ pF, $V_{\mathrm{dd}} = 3$ V, and $V_{\mathrm{range}} = 0.5$ V, the maximum attainable FOM is 0.7 conversions per picojoule (pJ) of energy. The experimental results confirm this FOM for the analog component of the dissipated power.

IV. EXPERIMENTAL RESULTS

The potentiostat system integrates 16 identical current input channels onto a single VLSI chip measuring 3×3 mm^2 in 0.5-μm CMOS technology. Fig. 8 depicts the micrograph and system floorplan of the chip. Voltage reference levels V_{ref} are set individually for 4 groups each comprising 4 channels. Reference current I_{ref} of the feedback DAC, gain G and oversampling ratio OSR are set jointly for all 16 channels.

The power supply voltage is 3 V, with V_{mid} set to 1.5 V, and cascode biases set for a signal swing of 2.4 Vpp at the cascoded inverting amplifier output. These biases were provided off-chip for test purposes and would incur a small area and power penalty when integrated on-chip. For implantable use, it would also be necessary to generate reference voltages V_{ref} and reference current I_{ref} using on-chip D/A converters. A single clock and configuration bit sequence generates all clock signals internally. The output is read asynchronously in bit-serial form using a separate clock.

A. Chip Characterization

For performance characterization of the potentiostat chip, multiple input current sweeps were performed using a Keithley SourceMeter model 6430 (Keithley Instruments Inc., Cleveland, OH) controlled via a GBIP interface. In the following tests, the system clock frequency f_s was set to 2 MHz, the DAC reference current I_{ref} was set to 500 nA, and the amplifier bias I_b was set to 200 nA. The input potential V_{ref} was set to 1 V. The digital gain G and oversampling ratio OSR were programmed individually for each test, varying between 1 and 2^{16}.

To verify the range and precision of the potentiostat at fixed value of the reference current, we swept the input currents logarithmicly over a range spanning over six orders of magnitude [14]. Fig. 9 [15] shows the normalized digital output of the chip as a function of input current. The normalization is necessary for comparison across various scales. The gain G, oversampling ratio OSR, and corresponding range of input currents I_{range}, conversion time $1/f_{\mathrm{conv}}$ and power dissipation P_{diss} are shown in Table I for each of the traces in Fig. 9. The value of the integrating capacitor C_1 was kept at 1.1 pF. In each consecutive sweep, the conversion time was doubled, while the value of current corresponding to the least significant bit was decreased four-fold illustrating the tradeoff between conversion speed and resolution of measurement. Fig. 10 shows the relation between the digitally programmed gain G and the actual measured gain [24].

The analog power consumption by the chip, covering all 16 integrators, 16 comparators, and bias circuits measured 53 μW, identical for each of the range selections in Fig. 9. We did not adapt the amplifier bias $(I_b = 200\ \mathrm{nA})$ with the value of digital gain G which would lead to further power savings at high G values. At 3.3 μW per channel, the resulting FOM is 0.6 conversions per pJ consistent with (14). The measured digital power consumption by the chip ranged from 1.2 mW for digital gain $G = 1$ down to 495 μW for gains larger than $G = 2^8$. This power measure covers clock generation and bit-serial readout in addition to the 16 decimators. Therefore, we anticipate the 495 μW asymptote of the measure excludes the array of decimators, and the digital power ranges between 0 and 44 μW per channel. Digital power consumption could be further reduced by low-power digital design techniques such as gray-level counters for the decimators.

To demonstrate the utility of digital gain by $1/G$ duty-cycle modulation of current feedback, we compared the sensitivity for digital gain G with that for an equivalent increase in oversampling ratio G OSR. The value of the integrating capacitor C_1

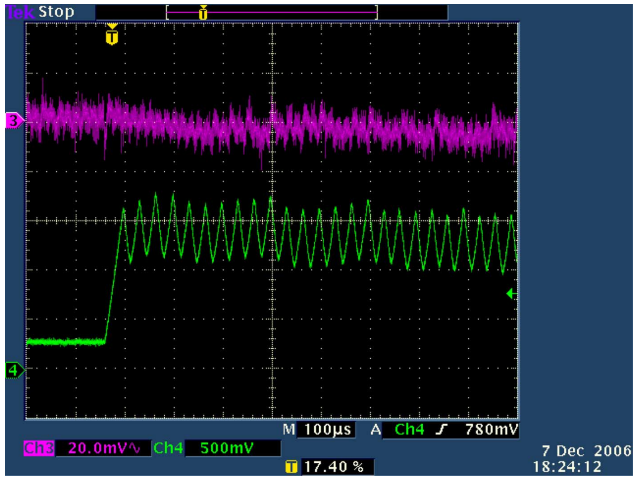

Fig. 12. Measured voltage variation Top: voltage at the input node, reset to $V_{\rm ref}$ at the beginning of the conversion cycle. Bottom: voltage at the output of the integrator.

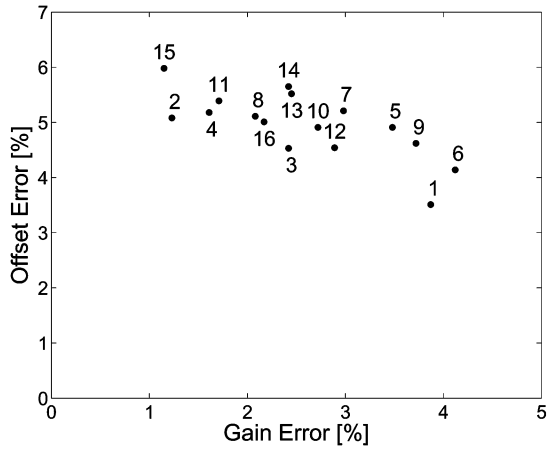

Fig. 13. Measured gain and offset errors, relative to nominal gain and offset values, across the 16 channels.

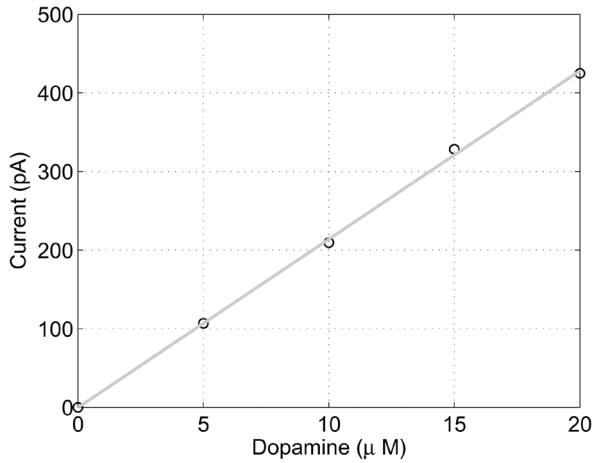

Fig. 14. Static current output of the potentiostat chip in response to additions of 5 μM dopamine.

was set at 0.1 pF and a current reference $I_{\rm ref}$ value was 256 nA. The input current was swept from $-$ 800 to 800 pA in steps of 2 pA. This sweep range covers the ± 1 nA range selected by a digital gain G set to 256. Over the same range, the input is observed at the same effective 8-bit resolution by the setting $G = 1$ and $\mathrm{OSR} = 2^{16}$. The integral nonlinearity (INL) measured for both settings of digital gain and oversampling ratio are shown in Fig. 11. As predicted in Section III, even though both settings have the same nominal resolution $1/G\mathrm{OSR}$, the setting with larger digital G gives lower error. The measured improvement in sensitivity in Fig. 11(a) over (b) is consistent with the $\sqrt{G}$-fold improvement predicted for $G = 256$. The instability in the center region of Fig. 11(b) is due to the small feedback capacitance $C_1 = 0.1$ pF and increased input capacitance of the autoranging sourcemeter instrument at its lowest scales.

To test the voltage clamping characteristic of the potentiostat, we observed the variation in input voltage,starting from reset of the capacitor C_2 sampling the reference voltage $V_{\rm ref}$. Fig. 12 shows the variation of voltage at the input node, and the corresponding variation at the output of the integrator. The digital gain G was set to 1 and oversampling ratio OSR was 2^{16}, leading to a conversion time of 16 ms.

Mismatch between channels was characterized by evaluating gain and offset errors across channels. The current was swept over the range ± 8 nA for $I_{\rm ref} = 2\ \mu$A, $G = 256$, and $\mathrm{OSR} = 2^{12}$. For each of the channels, the deviation from ideal gain and offset was computed and represented in relative units in Fig. 13. The variation is due to current mismatch in transistors $M1$ and $M2$, and could be reduced by careful layout techniques using centroid geometry and local current mirroring, at the expense of a two-fold increase in analog power consumption and significant additional silicon area. We opted instead for digital calibration and compensation of the gain and offset errors.

Comparison of our design with VLSI potentiostats in the literature indicates highest sensitivity at lowest power consumption per channel. The comparison of current sensitivity, dynamic range, number of channels and power consumption is summarized in Table II. The larger dynamic range and sensitivity of our design owes to the use of digital gain modulation.

B. *Neurotransmitter Measurements*

Following electrical testing and characterization of the potentiostat, we performed basic neurotransmitter measurements. The chip was used for potentiostatic measurements of the neurotransmitter Dopamine in a phosphate buffered solution (PBS). Lack of dopamine producing neurons is implicated in Parkinson disease [25]. A standardized solution of dopamine was prepared [10] to test the chip *in vitro*. A static calibration curve of the potentiostat output versus dopamine concentration was generated using commercial carbon fiber electrodes (CF30-250, WPI, Fl.). Different concentrations of dopamine were added to a stirred PBS and the chip output allowed to equilibriate. The volume of the PBS and the dopamine added were adjusted to obtain final concentrations in steps of 5 μM. A commercial Ag–AgCl electrode (Bioanalytical Systems, IN) was used as the reference. The result is shown in Fig. 14.

To test the chip in a more realistic situation where neurotransmitters are not static but flowing, we used a multielectrode flow sensor [26]. Fig. 15 shows the experimental setup with the potentiostat acquiring multichannel real-time dopamine concentrations from the microfabricated sensor array. Fig. 16 shows a multichannel multisite measurement of dopamine. Initially PBS

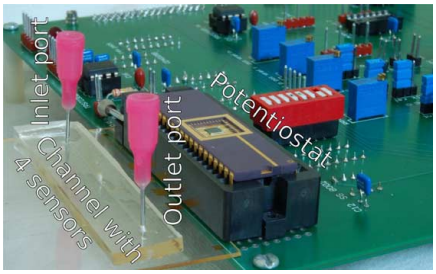

Fig. 15. Experimental setup showing the potentiostat chip interfaced to the multichannel flow sensor.

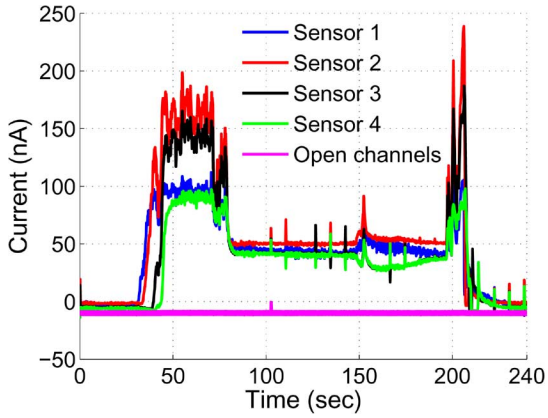

Fig. 16. Real-time 4 channel simultaneous monitoring of neurotransmitters flowing in a fluidic channel.

TABLE III
MULTICHANNEL POTENTIOSTAT CHARACTERISTICS

Technology	0.5 μm 2P3M CMOS
Size	3 mm × 3 mm
Supply	3 V
Current inputs	16
Current range	100 fA to 1 uA
Minimum detected current	100 fA
Power dissipation	
Array:	
Analog	4.3 uW / chan.
Digital	44/G uW/ chan.
Chip total	450 uW - 1.2mW

was pumped through the channel. At $t = 40$ s, the pumped solution was changed to a dopamine solution. This leads to the transient increase in the currents measured by the potentiostat. The responses of individual channels correspond to the order in which the sensors see the dopamine, with the first sensor being the one most upstream. At $t = 75$s, the pumping was stopped and the sensors transduce the static dopamine concentration into a relatively constant current. Pumping was restarted at $t = 150$ s and the pumping solution was changed back to PBS at $t = 200$ s. This leads to transient effects again and as the dopamine is washed out by the PBS, the currents return to the baseline levels.

V. CONCLUSION

We presented a 16-channel potentiostat array with a wide dynamic range of currents that span through six orders of magnitude from picoamperes to microamperes and sensitivity down to 100 fA. The current range is controlled through programmable feedback duty-ratio cycle. The measured characteristics are summarized in Table III. The potentiostat chip was used to acquire real-time multichannel data from a microfabricated neurotransmitter sensor array. Further tests and developments are validating the technology with wireless telemetry in an integrated implantable neurotransmitter monitoring system [17].

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