19.9 Temporal Change Threshold Detection Imager

Udayan Mallik, Matthew Clapp, Edward Choi, Gert Cauwenberghs, Ralph Etienne-Cummings

Johns Hopkins University, Baltimore, MD

Covert, low-power and low-bandwidth sensor networks for intelligent surveillance require imaging front-ends that make rudimentary decisions to perform or facilitate data compression. Typically, this front-end is composed of a standard Active Pixel Sensor (APS), an ADC and additional digital logic for image processing and communication control. As is expected, these systems are large (unless integrated) with considerable power budgets. To circumvent these problems, a CMOS imager that integrates circuits for basic decision-making and image compression on the focal plane is described. The chip is used as a low-power vision sensor and wake-up detector for these ad hoc networks.

At its core the chip is a 90×90 array of NMOS-only pixels that include both a Three transistor (3T) APS, and a 3T/2C 1.5b ADC for Change/Motion Detection (C/MD) (see Fig. 19.9.1). The compact C/MD circuit outputs events indicating the polarity of intensity changes at each pixel. It may also be used as a pixel-level ADC [1] for the APS image or the difference. A FIFO is filled with pixel address, APS value and C/MD event type when the intensity changes exceed pixel-specific levels. Presence of data in the FIFO signals changes in the environment; outputting only the changes realizes image compression. All imaging, signal conditioning and decision-making tasks are performed as Computation-On-Readout (COR) and are scalable to larger arrays without sacrificing real-time performance. Unlike previous change-coding imagers [2],[3],[4],[5], the present imager uses detected change events to gate transmission of APS readout, leading to efficient change coding as well as compression. Figure 19.9.7 is a micrograph of the chip. The light shielding layer occludes circuit details.

Overall chip layout and schematics showing the significant dataflow paths are illustrated in Fig. 19.9.1. All computations are performed following a column parallel architecture. Signal timing required for operating the chip, repeated at each row, is illustrated in Fig. 19.9.2. The image is produced using a standard 3T APS. Each column contains a Difference Double Sampling (DDS) circuit, for Fixed Pattern Noise (FPN) suppression. Closing 'S' samples both the integrated APS voltage (V_{aps}) across C1 and external voltage V_{ref} across C2. With 'apsReset' high and 'S' open, output of the cascoded common source amplifier establishes a feedback path with the input across the capacitors, subtracting the pixel reset voltage from the stored image (with DC offset V_{ref}), to produce a DDS video output.

The in-pixel C/MD circuit is composed of a comparator (3 NMOS transistors), a storage capacitor (C_{aps}) and a control capacitor (C_{comp}), as shown in Fig. 19.9.1. The comparator's PMOS active load is embedded in the edge circuit and shared by all pixels in a column (only one row is activated at a time). Once the column DDS circuit samples V_{aps}, it is "stored" on C_{aps} by closing the feedback switch M6 around the comparator. In the next frame, V_{comp} is switched above ($+dV_{comp}$) and below ($-dV_{comp}$), its resting level, to define a voltage "rejection band" and compare the new V_{aps} with these two threshold levels centred around the stored V_{aps}. If the new V_{aps} is lower than the previously stored voltage by a threshold ($-dV_{comp}$), comparator output is high in both comparison states. If it is higher than stored voltage by a threshold ($+dV_{comp}$) then comparator output is low in both comparison states, where $+dV_{comp}$ and $-dV_{comp}$ are test margins above and below the trip voltage of the comparator, respectively. Results are time multiplexed and stored in registers C+ and C-, respectively. Adjusting the control voltage, V_{comp}, during change detection compensates for leakage across the storage capacitor C_{aps} due to photocurrent on switch junctions, and signal-independent switch injection noise. The new V_{aps} is now stored on C_{aps} by closing M6, as before for the next cycle. The comparison bits form inputs to chip level 'XNOR' and 'AND' circuits to produce detection and type classification signals that gate the DDS output onto the FIFO. Performance metrics for the chip are tabulated in Fig. 19.9.3.

Figure 19.9.4 quantifies dependence of detection on the amplitude of intensity change as a function of symmetric test margin magnitudes under uniform but temporally changing luminance conditions. Vertical scale indicates fraction of pixels that respond with a detection. The spread of transitions is due to pixel and column transistor variations.

As a visual demonstration of classified ON/OFF temporal transient sensitivity, a rotating, radial and concentrically alternating flywheel pattern, placed in a cluttered static environment, was presented to the imager. The V_{comp} rejection band is set to be 2.3V±0.18V. In Fig. 19.9.5 from left to right, are the image, its detected edges while rotating at 3rev./s, and its edges when rotating at 1rev./s, respectively. Note that the static background does not trigger any detection.

Figure 19.9.6 shows the reconstruction performance of the algorithm at two different test margin settings for a given natural scene. For images (b) and (e) the V_{comp} rejection band is set to 2.3±0.1V, while in (c) and (f) it is set as 2.3±0.15V, to reduce bandwidth allocation for the same scene. Images (a) and (d) are frames 33 and 77 in the sequence. Figures 19.9.6 (b) and Fig. 19.9.6 (c), display DDS values at all pixel addresses that detect intensity change greater than the set threshold during transition between frames 76 and 77. In each frame the old DDS values of pixels at addresses indicating a change are replaced with new DDS values. Images (e) and (f) display the reconstructed scene at frame 77, after evolving through successive frame-to-frame updates in the two experiments.

Acknowledgments:
The chip was fabricated through the MOSIS Educational Program (MEP) as part of a VLSI class project. The authors thank Dr. Viktor Gruev for his insight during testing.

References:
[1] D. Yang, B. Fowler and A. El-Gamal, "A Nyquist-Rate Pixel-Level ADC for CMOS Image Sensors," *IEEE J. Solid-State Circuits*, vol. 34 (3), pp. 348-356, March, 1999.
[2] J. Kramer, "An On/off Transient Imager with Event-Driven, Asynchronous Readout," *IEEE ISCAS,* vol. II, pp 165-168, May, 2002.
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[5] A. Dickinson et al., "A 256×256 CMOS Active Pixel Image Sensor with Motion Detection," *ISSCC Dig. Tech. Papers* pp. 226-227, Feb., 1995.

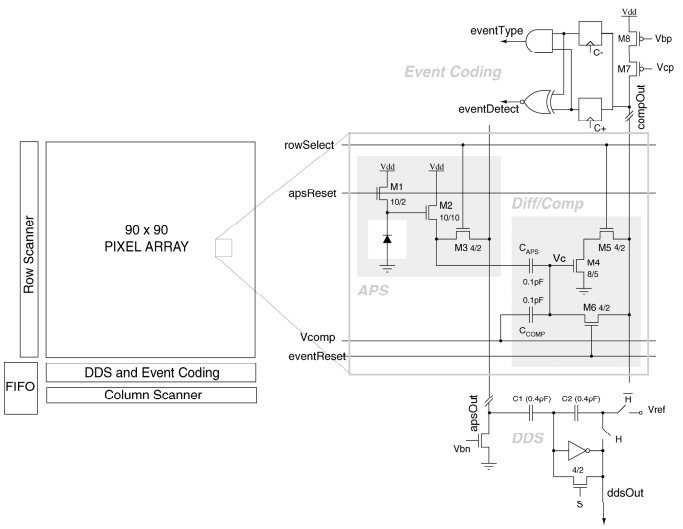

Figure 19.9.1: Chip system diagram and circuit schematics.

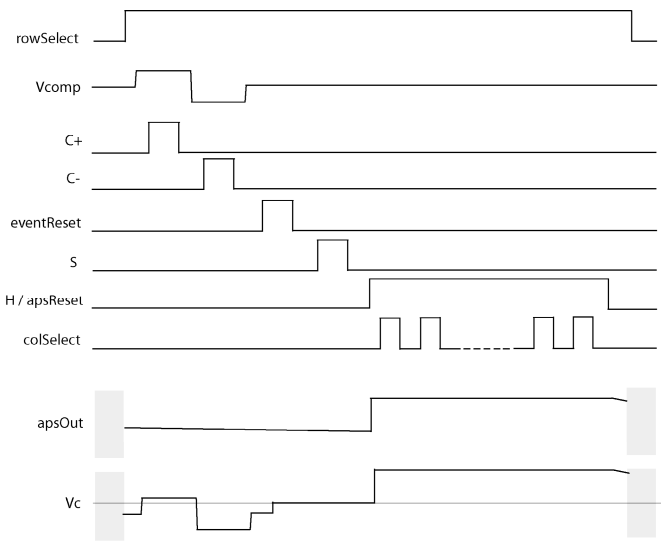

Figure 19.9.2: Timing diagram for chip operation.

Technology	0.5um 3Metal 2Poly CMOS
Die Size	3mm by 3mm
Pixel Size	25.2um by 25.2um
Fill Factor	17%
FPN	0.5% @ 30fps
Dynamic Range	~51dB
Change Sensitivity	2.1% per Frame @ 1.7uW/cm^2
Power Consumption	4.3mW @ 3V and 30fps

Figure 19.9.3: Chip parameters and performance.

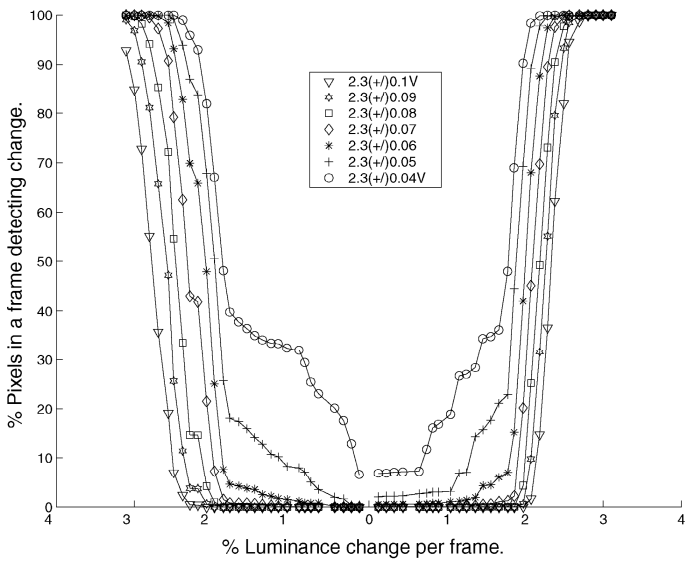

Figure 19.9.4: Sensitivity plots for various rejection bands.

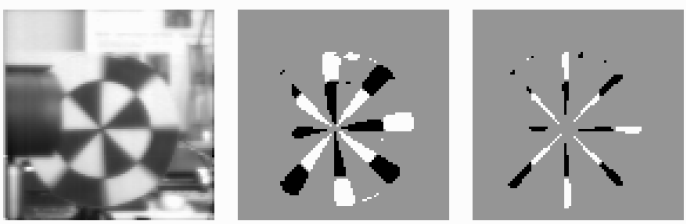

Figure 19.9.5: Fast and slow rotating flywheel edges.

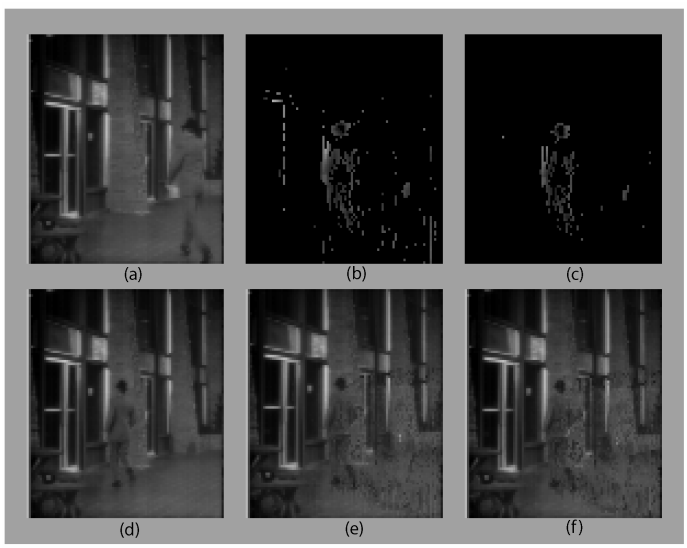

Figure 19.9.6: Compression performance.

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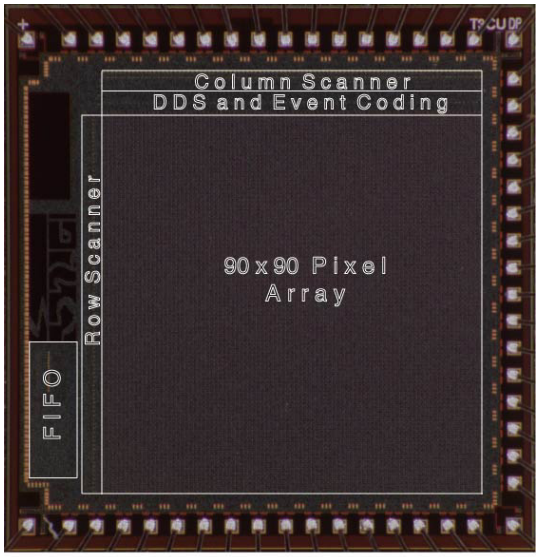

Figure 19.9.7: Chip Micrograph.

