A Floating-Gate Programmable Array of Silicon Neurons for Central Pattern Generating Networks

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***Abstract*— A new central pattern generator chip with 24 silicon neurons and reprogrammable connectivity is presented. The 3mm $\times$ 3mm chip fabricated in a 3M2P 0.5μm process contains 1032 synapses, each with multiple floating gates for storing parameters governing synaptic strength and polarity. Every neuron includes a dendritic compartment with 12 externally-addressable synaptic inputs and 24 recurrent synaptic inputs, enabling construction of a fully-interconnected network with sensory feedback from off-chip elements. In addition to describing the chip architecture and neuron circuits, preliminary results from single oscillating neurons and pairs of phase-locked neurons are shown. This work represents the realization of a design presented at ISCAS'05, and an improvement over our 2nd generation CPG chip presented at ISCAS'04.**

I. Introduction

Central pattern generators (CPGs) are small, semi-autonomous networks of neurons that produce rhythmic patterned outputs to control motor functions. CPGs have been found in all organisms studied, from invertebrates [1] to vertebrates [2] and, recently, humans [3]; they are responsible for behaviors such as flying, swimming, chewing, walking, breathing, and other regular activities [4], [5]. Although typically not necessary for basic functionality [6], sensory feedback and descending inputs from the brain are normally used to modulate and control the CPG output [7].

The goal of this work is to develop a silicon analog of the biological central pattern generator to control locomotion in robots and, potentially, to serve as an *in vivo* replacement for a real CPG after spinal cord injury. A number of silicon CPGs can be found in the literature [8]–[11] with varying degrees of biological realism. Chips with the most sophisticated neural models [8] are based on the Hodgkin-Huxley formalism and generate realistic spike outputs. However, these neurons occupy a large silicon area and are not well-suited to large-scale integrated networks. The use of simple integrate-and-fire models allows for implementation of many neurons on the same silicon die [9], but forgoes the realistic dynamics that may be useful in generating complex output patterns.

Our previous CPG chip [9] allowed for 10 silicon neurons to be fully interconnected via digitally-controlled synapses. This architecture was used to create oscillatory networks with sufficient complexity to control a bipedal robot [12]. However, the digital-to-analog converters employed to store the synaptic strengths occupied a large on-chip area and required programming each time the chip was powered on. More recently, we presented a design for compact synapses using non-volatile analog storage on floating-gate (FG) transistors [13]. We have now fabricated and begun to test a chip (Fig. 1) that integrates 1032 of these FG synapses in an array of 24 silicon neurons.

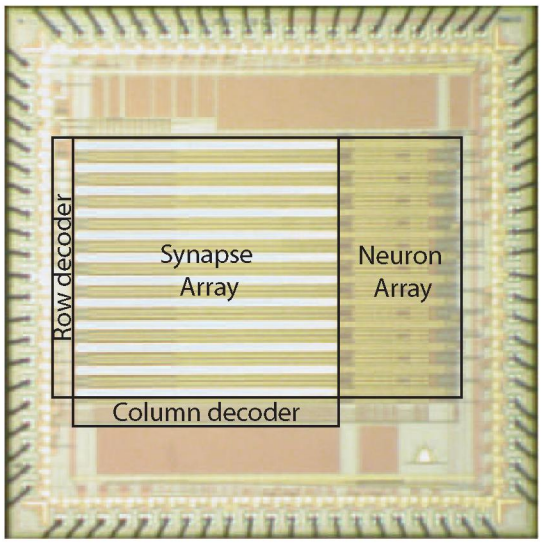

Fig. 1. Micrograph of the 3mm $\times$ 3mm FG-CPG chip fabricated in a 3M2P 0.5 μm process.

II. Chip Architecture

The floating-gate central pattern generator (FG-CPG) chip architecture is similar to that described in [9], [13], and is illustrated in Figure 2. Twenty-four identical silicon neurons are arranged in rows, with 12 external inputs and 24 recurrent inputs running in columns across the chip. Each of the 36 inputs makes synaptic connections to all 24 neurons via the floating-gate synapse circuits described in Section II-A (Fig. 3). In addition to the external and recurrent inputs, neurons also receive a bias current from a simple current mirror (not shown).

A. Neuron Circuit

A block diagram of the neuron subcircuit is shown in Figure 4. As mentioned in [13], these cells have three differ-

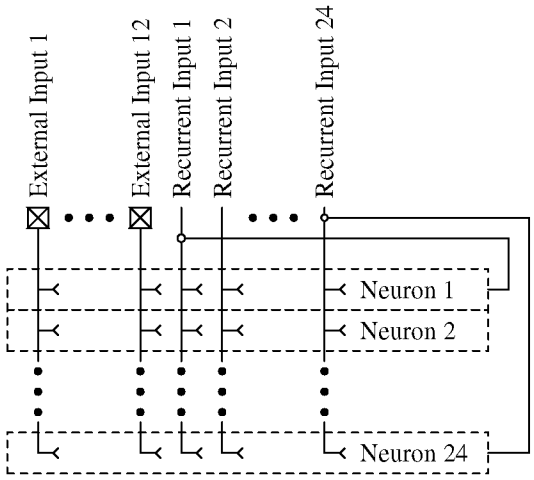

Fig. 2. The FG-CPG chip floorplan. Twenty-four silicon neurons are arranged in rows, and thirty-six inputs are arranged in columns. A floating-gate synapse is located at the intersection between each input and neuron. The first 12 inputs are "external" in the sense that they are gated by off-chip signals; the remaining 24 inputs are gated by the outputs of the 24 on-chip neurons and are therefore called "recurrent". A fully-interconnected network can be created by activating all of the recurrent synapses.

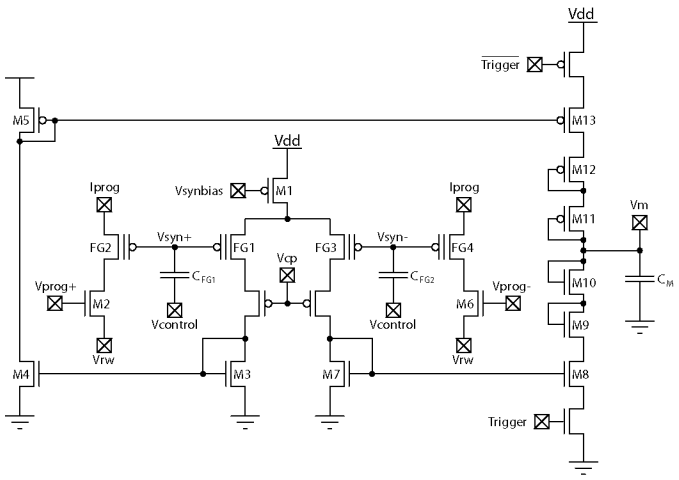

Fig. 3. Floating-gate synapse circuit schematic. Each synapse contains nonvolatile analog memory elements for storing a differential voltage on the gates of FG1–FG4, which determines the strength and polarity of the synapse.

ent compartments—dendritic, somatic, and axonal—that are both functionally and spatially distinct. In Figure 1, it can be seen that the dendritic compartments (labeled "synapse array") occupy most of the silicon area, while the somatic and axonal compartments (labeled "neuron array") are relatively smaller. This is partially due to the large number of synapses implemented, but mostly because the membrane capacitance is distributed throughout the dendritic compartment to achieve a compact layout. The contents of the neuronal compartments are described briefly below:

- The dendritic compartment contains 12 external and 24 recurrent synapses, where each synapse is implemented with the floating-gate circuit described in Section II-B. For testing purposes, a bias current can also serve as an input to the neuron.
- The somatic compartment contains a large capacitor (modeling the membrane capacitance of a biological neuron), a hysteretic comparator (modeling the axon hillock), and some specialized "synapses" that discharge the cell and implement a refractory period.
- The axonal compartment contains specialized "synapses" that produce variable-duration spike outputs and allow for spike-frequency adaptation. The spike outputs are buffered and sent off-chip to control external motor systems, and are also used to gate the 24 recurrent synapses between each cell, all of its neighbors, and itself.

Although all three compartments of the neurons contain the same synapse circuit (Sec. II-B), only the 36 dendritic inputs are synapses in the traditional sense. Programmable current sources used to reset the neuron and implement a refractory period, spike-width modulation, and spike-frequency adaptation are implemented with a floating-gate synapse circuit only for convenience.

B. Synapse Circuit

The 1032 on-chip floating-gate synapses (including external, recurrent, and specialized synapses) are all implemented with a simple nine-transistor operational transconductance amplifier (OTA), similar to that presented in [13] (Fig. 3). Briefly, hot-electron injection (HEI) [14] and Fowler-Nordheim tunneling [15] are used to add and remove charge from C_{FG1} and C_{FG2}, creating a differential voltage for the OTA and thereby setting the current through M13 and M8. When the synapse is activated by placing a digital high voltage on $Trigger$ and a low voltage on $\overline{Trigger}$, this differential current flows through C_M and affects the membrane potential V_m. If V_{syn+} is less than V_{syn-}, the synapse will be excitatory and add charge to C_M; inhibitory synapses are created by setting V_{syn+} greater than V_{syn-}. Because Fowler-Nordheim tunneling requires high voltages, HEI is used for most programming tasks—changes in synaptic strength and polarity are both achieved by varying the *differential* OTA voltage—and tunneling is reserved for "resetting" the synapses when the absolute voltage on a floating gate reaches zero. One notable improvement of this synapse circuit over the design presented in [13] is the addition of the $V_{control}$ node, which allows for increased programming range and better control of the voltage on the floating gates.

III. Results

Figure 5 shows preliminary data recorded from a single on-chip neuron. The neuron is oscillating due to a constant influx of bias current in its dendritic compartment. By adjusting the bias input, it is possible to achieve a wide range of spike frequencies, from approximately 1 Hz to 150 kHz. The maximum and minimum values of the membrane potential are set by the somatic compartment's hysteretic comparator; through appropriate tuning of the comparator's midpoint and tail current, it is possible to make the charging and discharging nonlinear due to the diode-connected transistors at the

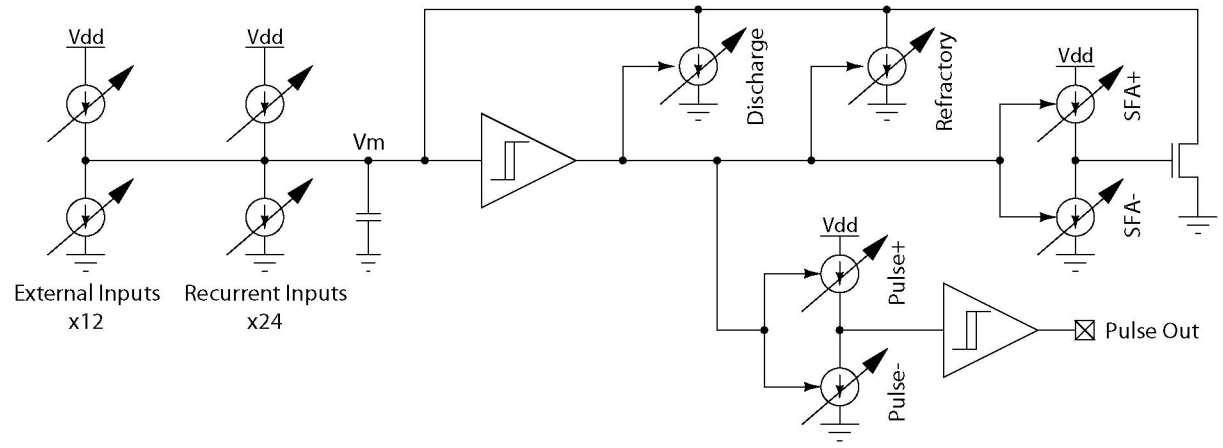

Fig. 4. Block diagram of our silicon neuron. Including the specialized "synapses" for discharging the cell and implementing a refractory period, pulse width modulation, and spike-frequency adaptation, each neuron contains 43 floating-gate synapses (drawn as an individual or pair of adjustable current sources).

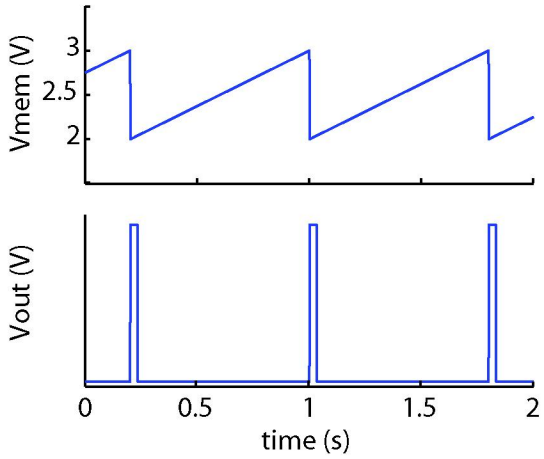

Fig. 5. A single neuron can be made to oscillate by injecting a small bias current onto its membrane capacitor. (Top) Oscilloscope output displaying neuron's membrane potential. (Bottom) Oscilloscope output displaying neuron's pulse outputs. The pulse width is relatively short here, but can be adjusted over a wide range of values by programming the specialized pulse width "synapse" (Sec. II-A).

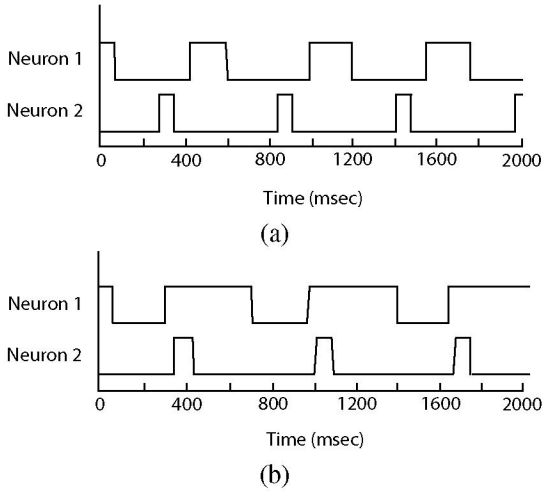

Fig. 6. Oscilloscope output displaying phase-locked neurons with different phase offsets and pulse widths.

synapses' output node (M9–M12 in Figure 3). The benefits of this nonlinearity have been explored in our previous work [9], [12], [13].

In order to generate useful signals for locomotion, a central pattern generator must be able to generate phase-locked outputs. Figure 6 illustrates two examples of phase-locking using neurons from the FG-CPG chip. In both cases, each neuron received excitatory input from an external synapse and inhibited the other neuron through a recurrent synapse. Phase delays were created by varying the synaptic strength of the external input. Figure 6 also shows an example of how the specialized pulse width "synapse" can be used to increase or decrease the duration of the neuron's output. The ability to create variable-duration outputs with arbitrary phase relationships is important when the CPG is used to control locomotion with multiple flexor/extensor pairs. For example, the onsets of hip and knee actuators are typically 90° degrees out-of-phase, and the duration of hip activation is approximately twice as long as knee activation [16].

IV. Conclusion

Our preliminary results demonstrate the functionality of our 3rd generation central pattern generator chip. By replacing the bulky digital-to-analog converters in our previous design [9] with compact floating gate circuits, we were able to increase the number of neurons and synapses by 85% and 261%, respectively, for an equivalent silicon area. Additionally, the chip is more versatile than the previous design: as the the tail currents on the synapse OTAs are varied from subthreshold currents to large suprathreshold currents, the neurons generate oscillations over six orders of magnitude in the frequency domain.

We are currently working to create complex networks sufficient to produce locomotion in a robotic biped. Previously, we presented a network of twelve neurons that can control

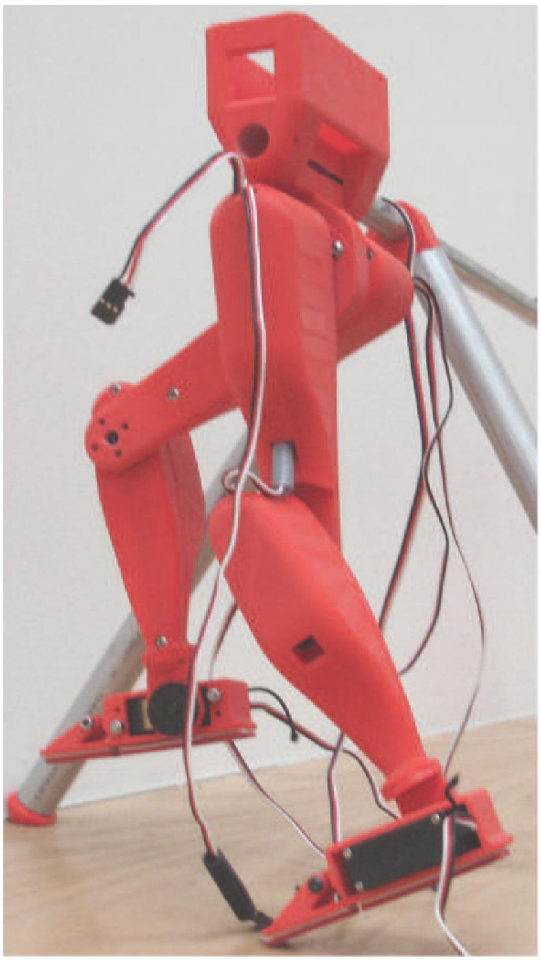

Fig. 7. The RedBot robot (courtesy Iguana Robotics Inc., Urbana, IL, USA).

bilateral hip and knee extensors and flexors [16], and can be extended to control robotic feet, as well (unpublished). Application of appropriate sensory feedback should allow for stable output patterns in the presence of perturbations such as those occurring during overground walking [17]. We therefore intend to implement this network on a single FG-CPG chip and use it to control the RedBot robot (Fig. 7).

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