CHARGE-BASED MOS CORRELATED DOUBLE SAMPLING COMPARATOR AND FOLDING CIRCUIT

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ABSTRACT

A novel charge-based comparator and folding circuit are presented. Correlated double sampling comparison is performed using a log-domain integrator, implemented by a subthreshold nMOS transistor with the source coupled to a capacitor. The circuit produces a current that is a logistic function of the change in voltage on the gate, with an input-referred offset voltage that is a logarithmic function of time. Folding operation for analog-to-digital conversion is obtained by differentially combining currents from a bank of these comparators. A prototype 128-channel parallel 4-bit gray-code analog-to-digital converter has been implemented in a 0.5 μm CMOS process, delivering 128 MS/sec at 76 mW power dissipation.

1. INTRODUCTION

High-performance data conversion can be achieved either by expending power and area to achieve high precision in a single analog architecture, or by distributing the architecture over multiple low-resolution quantization tasks each implemented with relatively imprecise analog circuits, and combined in the digital domain. The latter approach has proven superior in attaining very high precision, by distributing the quantization process over time using delta-sigma modulation [1]. Both high speed and high resolution can be achieved by distributing the quantization process in space. To this end, it is necessary to implement very space efficient, low-resolution quantizers.

We present a charge-based circuit that implements an offset-compensated comparator with one capacitor and four nMOS transistors. Besides applications in data conversion, the design targets applications in hybrid analog-digital computing using large-scale analog arrays [2], where parallelism, redundancy in information representation, and statistical data coding [3] can be used to compensate for imperfections in analog sensing and computation.

2. CHARGE-DOMAIN CORRELATED DOUBLE SAMPLING COMPARATOR

2.1. Capacitor-nMOS Integrator

To obtain high density and high speed in a comparator and folding circuit, the challenge is to design a single stage producing a current-mode or charge-mode signal that is a saturating high-gain and offset-compensated function of a difference in input voltage. We show that in the charge domain this can be achieved using a circuit incorporating a capacitor and an exponential element, such as a diode [4] or a MOS transistor operating in subthreshold regime [5], where the differential voltage is presented as an initial condition at the input. Offset compensation is achieved in the charge domain, as for the CMOS charge-transfer comparator described in [6].

In the circuit of Figure 1*(a)* the nMOS transistor is source coupled to a capacitor. In the subthreshold and saturation region, the drain current is exponential in gate and source voltage, and the large-signal dynamics of the integrator are described by:

$$C\frac{dV_s}{dt} = I_s = \frac{W}{L} I_o e^{(\kappa V_g - V_s)/V_t}, \tag{1}$$

where V_t is the thermal voltage. Integrating the differential equation (1) yields:

$$CV_t e^{\frac{V_s}{V_t}} = \frac{W}{L} I_o e^{\kappa V_g / V_t} t + c_1, \tag{2}$$

where c_1 is an integration constant. Direct substitution yields:

$$I_s(t) = \frac{CV_t}{t + \frac{c_1}{\frac{W}{L} I_o e^{\kappa V_g / V_t}}}. \tag{3}$$

At time $t = 0$, the input voltage is switched from $V_g(0^-)$ to $V_g(0^+)$ while the capacitor instantly retains the source voltage $V_s(0)$. The source current therefore switches from $I_s(0^-)$ to $I_s(0^+)$ over the transition at the gate:

$$I_s(0^+) = I_s(0^-) e^{\kappa \triangle V_g / V_t}, \tag{4}$$

where $\triangle V_g = V_g(0^+) - V_g(0^-)$. The output current (3) can thus be expressed in terms of initial conditions:

$$I_s(t) = \frac{I_s(0+)}{\frac{I_s(0+)}{CV_t} t + 1} = \frac{I_s(0-)}{\frac{I_s(0-)}{CV_t} t + e^{-\kappa \triangle V_g / V_t}}. \tag{5}$$

Interestingly, for $t \gg CV_t / I_s(0^+)$, $I_s(t)$ becomes independent of initial conditions:

$$I_s(t) \approx \frac{CV_t}{t}. \tag{6}$$

2.2. Comparator

Saturation of the output current of the circuit in Figure 1*(a)* as a function of a change in the input voltage V_g is utilized in the design of the charge-based comparator as shown in Figure 1*(b)*. The

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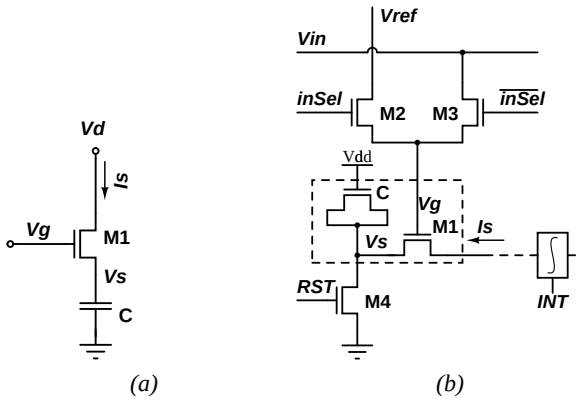

Figure 1: *(a) Capacitor-nMOS integrator and (b) charge-based comparator.*

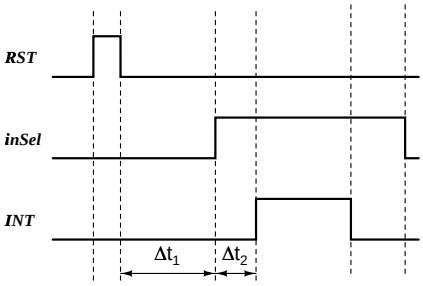

Figure 2: *Control signal timing diagram for the comparator circuit in Figure 1 (b).*

nMOS capacitor is initially charged by pulsing RST as shown in Figure 2. Over a time interval $\triangle t_1$, the capacitor discharges to raise V_s until $M1$ reaches well into the subthreshold region. The end of the interval defines the initial condition for the source current $I_s(0^-)$. The differential input voltage is presented as a transient on the gate, $\triangle V_g = V_{\rm ref} - V_{\rm in}$, implemented using an analog multiplexer M2-M3 and controlled by $inSel/\overline{inSel}$ timing signals in Figure 2. In subthreshold[1], this gate voltage transition produces a change in source current according to (5). By combining equations (4) and (5), the input-output characteristic of the comparator can be expressed as:

$$I_s(t) = I_{sat}\ \sigma\Big(A(\triangle V_g - V_{\rm off}(t))\Big), \tag{7}$$

where

$$\sigma(x) = \frac{1}{1+e^{-x}} \tag{8}$$

is a logistic function, the amplitude saturates to $I_{sat} = CV_t/t$, the voltage is scaled by $A = \kappa/V_t$, and the offset voltage

$$V_{\rm off}(t) = \frac{V_t}{\kappa} log \frac{CV_t}{I_s(0^-)t} \tag{9}$$

is a logarithmic function of time. Note that by virtue of *correlated double sampling* in the differential transient $\triangle V_g$ by switching M2-M3, the offset $V_{\rm off}(t)$ is independent of M1 threshold variations and, to first order, $1/f$ noise.

[1]For large values of $\triangle V_g$, the nMOS may initially enter the strong inversion region. This affects the timing but not the operation of the circuit, since once the capacitor has raised V_s to reach subthreshold, the asymptotic relationship (6) holds again.

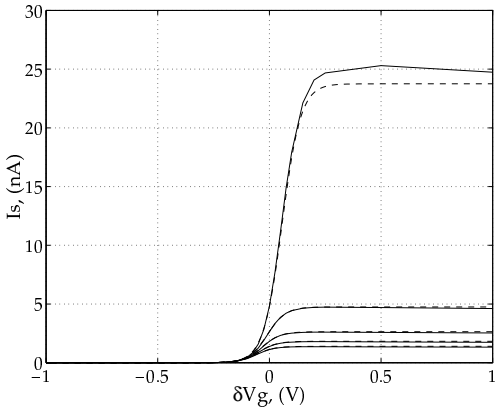

Figure 3: *The input-output characteristics of the charge-based comparator at different fixed time intervals $\triangle t_2$ after switching the inputs, calculated using equation (7) (dashed line) and simulated using SpectreS for a 0.5 μm CMOS process (solid line). (Top to bottom: $\triangle t_2$ = 50, 250, 450, 650, 850 ns.)*

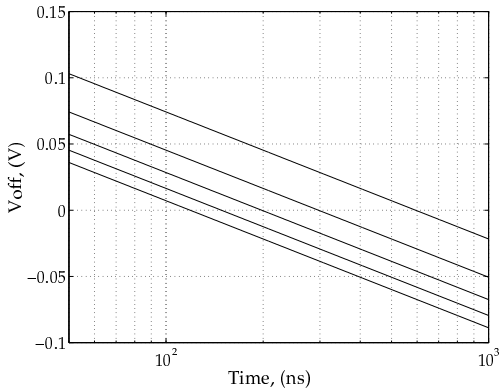

Figure 4: *The offset voltage of the comparator as a function of time after switching the inputs ($\triangle t_2$ in Figure 2). Theoretical results obtained using equation (9) for different values of $I_s(0^-)$. (Top to bottom: $I_s(0^-)$ = 2, 4, 6, 8, 10nA.)*

Figure 3 illustrates the input-output characteristics of the comparator for different time interval $\triangle t_2$ after switching the inputs, calculated using equation (7) and simulated using SpectreS for a 0.5 μm CMOS process. The offset of the comparator as a function of time from (9) is plotted in Figure 4. It scales logarithmically in time. It also depends on $I_s(0^-)$ which is controlled by the time interval, $\triangle t_1$, between the moment $V_{\rm in}$ is applied (after the reset) and the time $V_{\rm ref}$ is presented to the gate of $M1$. Figure 5 illustrates theoretical and simulated source current transients for different values of $\triangle V_g$.

3. CHARGE-BASED FOLDING CIRCUIT AND GRAY-CODE ADC

Several solutions for gray-code and charge-based A/D conversion exist. Conventional folded differential logic [7] (FDL) can elimi-

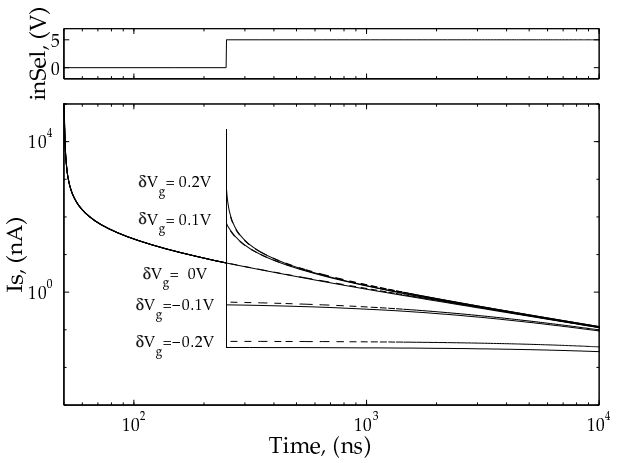

Figure 5: *Comparator output current transients for different values of $\triangle V_g$. The solid line shows the SpectreS simulation results for a 0.5 μm CMOS process; the dashed line was obtained using equation (7). The initial current $I_s(0^-) = 6nA$. Effective nMOS capacitor value is 45fF.*

nate code errors due to its wired gray-code encoding scheme. An improvement of FDL, folding cascoded differential logic (FCDL), was introduced in [8]. It allows for higher number of comparators in an encode block.

3.1. Gray-Code Flash ADC Architecture

Figure 6*(a)* shows the architecture of a 3-bit gray-code differential logic ADC. Comparators produce the output current

$$I_s^n = I_b((f(V_{\rm ref}^n - V_{\rm in}) + 1)/2), \qquad (10)$$

where I_b is a bias current, ${V_{\rm ref}}^n$ is a respective reference voltage level between ${V_{\rm ref}}^{\rm min}$ and ${V_{\rm ref}}^{\rm max}$, $n = 1, ..., 7$, and $f(.)$ is a decision function such as $\mathrm{sign}(.)$ or a logistic function. Each output bit, $D_i, i = 0, ..., 2$, is obtained by connecting comparator outputs differentially in a folding circuit, and then comparing the accumulated differential currents. The input-output characteristics of the ADC are illustrated in Figure 6*(b)*.

3.2. Folding Circuit

An LSB folding circuit for a 5-bit flash ADC is shown in Figure 7. The output currents can be expressed as:

$$I_+ = I_{sat} \sum_{n=0}^{(N-1)/4} \sigma\big(A(V_{\rm in} - V_{\rm ref}^{4n+1} - V_{\rm off}(t))\big), \qquad (11)$$

$$I_- = I_{sat} \sum_{n=0}^{(N-1)/4} \sigma\big(A(V_{\rm in} - V_{\rm ref}^{4n+3} - V_{\rm off}(t))\big) + I_b/2, \qquad (12)$$

where

$$I_b = I_{sat}\sigma\big(A(V_{\rm ref}^{\rm max} - V_{\rm ref}^{\rm min} - V_{\rm off}(t))\big). \qquad (13)$$

Theoretical and simulated output currents as a function of the input voltage for a folding circuit of a flash ADC are demonstrated in Figure 8.

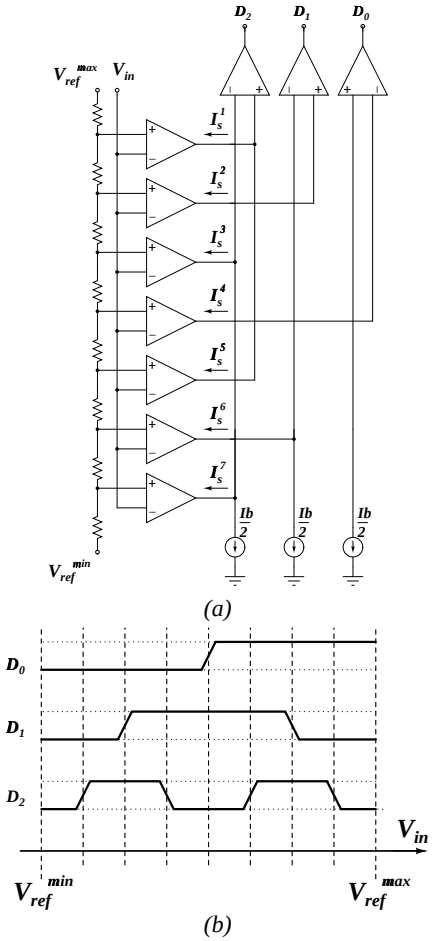

Figure 6: *A 3-bit gray-code flash A/D converter: (a) architecture; (b) characteristic.*

3.3. Integrating Sense Amplifier

Bit decisions are made on integrated, differentially folded comparator currents using a regenerative sense amplifier. Integration starts at the end of the $\triangle t_2$ interval, timed by the INT clock signal in Figure 2. The time-dependent comparator voltage offset (9) is inconsequential to the integration as it is in common to all comparator cells.

4. EXPERIMENTAL RESULTS

A prototype 128-channel 4-bit charge-based gray code ADC was fabricated in a 0.5 μm CMOS process. The die micrograph is shown in Figure 9. The chip contains, besides the parallel bank of flash ADCs, a massively parallel mixed-signal computational array [9]. The ADC bank measures 0.75 mm × 2 mm, and dissipates 76 mW of power at 128 MS/sec sampling rate. Output waveforms for a ramp input signal are presented in Figure 10.

5. CONCLUSIONS

A new charge-based comparator and a folding circuit have been reported. Each comparator performs correlated double sampling

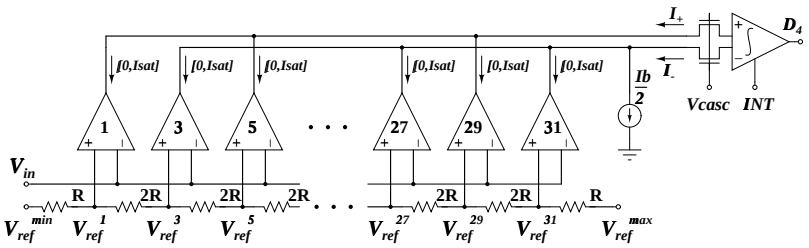

Figure 7: *Folding circuit for a charge-based gray code flash ADC.*

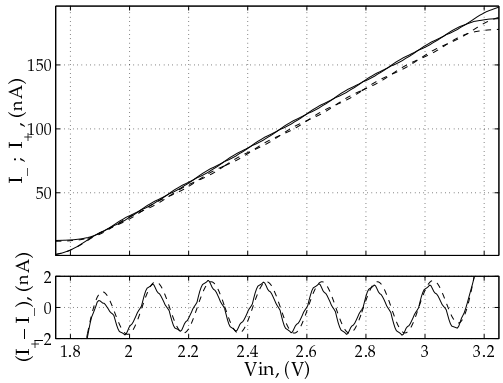

Figure 8: *Output currents of the folding circuit of Figure 7. The solid line represents the SpectreS simulation results for a 0.5 μm CMOS process; the dashed line corresponds to equations (11) and (12). The time interval $\triangle t_2$=50 ns.*

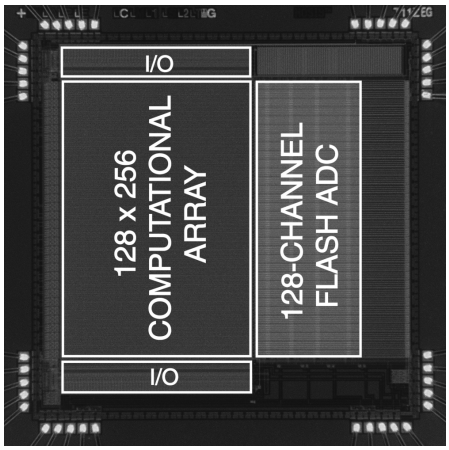

Figure 9: *Micrograph of a mixed-signal processor containing a computational array and a 128-channel parallel 4-bit gray-code flash analog-to-digital converter. Die size is* $3\ \mathrm{mm} \times 3\ \mathrm{mm}$ *in 0.5 μm CMOS technology.*

of the inputs to avoid mismatch errors. The circuit operates in weak inversion and yields both high speed and low power. The design is suited for parallel data conversion on mixed-signal computational arrays, active pixel imagers, and other distributed charge or voltage mode circuits. A prototype 128-channel parallel 4-bit gray-code analog-to-digital converter has been implemented in a

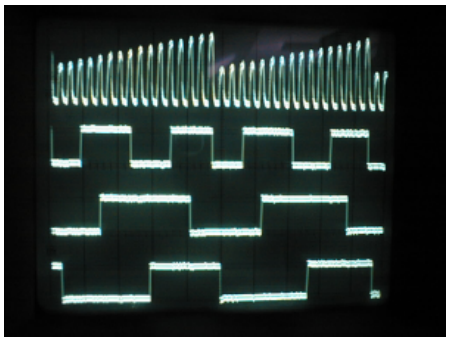

Figure 10: *Recorded gray-code flash ADC output waveforms as a function of input voltage.*

0.5 μm CMOS process, delivering 128 MS/sec at 76 mW power dissipation. It is trivial to extend the circuit with bipolar junction transistors for use in RF ADCs.

6. REFERENCES

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