A Subthreshold aVLSI Implementation of the Izhikevich Simple Neuron Model

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Abstract

We present a circuit architecture for compact analog VLSI implementation of the Izhikevich neuron model, which efficiently describes a wide variety of neuron spiking and bursting dynamics using two state variables and four adjustable parameters. Log-domain circuit design utilizing MOS transistors in subthreshold results in high energy efficiency, with less than $1pJ$ *of energy consumed per spike. We also discuss the effects of parameter variations on the dynamics of the equations, and present simulation results that replicate several types of neural dynamics. The low power operation and compact analog VLSI realization make the architecture suitable for human-machine interface applications in neural prostheses and implantable bioelectronics, as well as large-scale neural emulation tools for computational neuroscience.*

1. Introduction

Mathematical modeling of neural dynamics has been an invaluable tool in analyzing the behavior of neurons since its introduction by Hodgkin and Huxley more than fifty years ago [1]. Analog VLSI implementations of the Hodgkin-Huxley neuron formalization [2], while able to emulate a wide variety of neuron behaviors, also require a complex implementation and a large number of model parameters. The difficulty in realizing the complex functional form of the Hodgkin-Huxley model has motivated alternative realizations through simplifications that abstract the essence of integrate-and-fire dynamics at the cost of reduced ability to emulate a wide variety of neuron behaviors [4]. One model with particularly low implementation complexity and high model fidelity was recently formulated by Izhikevich [5], which emulates the dynamics of a wide range of neuron types using a compact representation of two state variables and four adjustable parameters. The various neuronal dynamics that this model can re-create are shown in Fig 1.

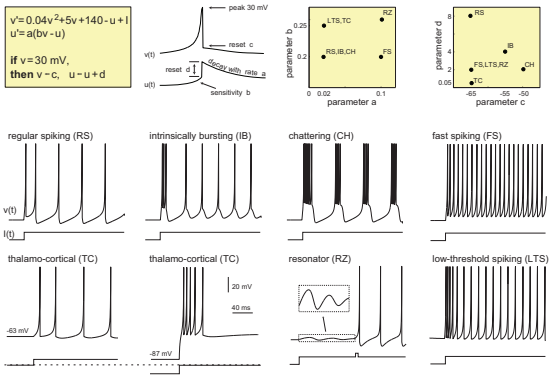

Figure 1. Dynamics of the Izhikevich simple model of the neuron [6]

A recent paper [7] utilizes the voltage mode approach to implement the Izhikevich simple neuron model and has a high power consumption.

We present the design and analysis of a current mode subthreshold MOSFET implementation of the simple model. The current mode approach has been proven to be low power, compact and relatively easy when compared to the voltage mode.

We will refer the interested reader to excellent treatises on the subject [8, 9, 10] and concentrate on the application of this theory to the simple model. The reader is introduced to the simple model in Section 2. Section 3 covers the detailed architecture and design. Closed form solutions are derived for the small signal transient behavior of the circuit. Simulation results are presented

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along with a discussion of the results in Section 4.

2. Simple Model

The phase plane of the equations lie in multiple quadrants depending on the mode of operation. This substantially complicates the circuit design by requiring the use of differential circuit topologies to represent both positive and negative state variables. Instead, a translation of the entire phase plane can be made to the first quadrant, simplifying the resulting design without affecting the dynamics of the circuit. The circuit design thus assumes all state variables are positive currents and will never go negative. From an analysis of the nullclines of the system, we can derive an approximate minimum for the membrane voltage to be 90mV which with margin can be assumed to be about 100mV. The a parameter will be assumed to be 0.02 while the b parameter will be set to 0.2. A MATLAB analysis of the original equations shows minimal changes in the dynamics of the circuit for these changes which lie within the typical design tolerances for a subthreshold circuit. Assuming all currents are in pico-Amps to minimize power consumption, we can convert the two state variables (v, u) to currents (I_v, I_u) as follows:

$$v = I_v - 100 \text{ and } u = I_u - I_o \tag{1}$$

where $I_o = b \times 100$

For reference, the original Izhikevich equations are shown below ($\tau = 1ms$ assumed in the model):

$$\tau \dot{v} = 0.04v^2 + 5v + 140 + I_{dc} - u \tag{2}$$

$$\tau \dot{u} = a(bv - u) \tag{3}$$

$$\text{If } v \geq v_{pk} \text{ then } \begin{cases} v \leftarrow c \\ u \leftarrow u + d \end{cases} \tag{4}$$

Substituting (1) into (2) and (3),

$$\tau \dot{I}_v = a_2 I_v^2 + a_1 I_v + a_0 + I_{dc} - I_u \tag{5}$$

$$\tau \dot{I}_u = ab I_v - a I_u \tag{6}$$

where $a_2 = 0.04$, $a_1 = 3$, $a_0 = 40 - b \times 100$.

3. Neuron Architecture

The circuit design utilizes a four transistor log domain filter [8] as the building block with MOSFET's biased in the subthreshold region. The drain current for this region of operation, I_D is an exponential function of the gate-source voltage V_{GS}:

$$I_D \approx I_0 \frac{W}{L} \exp\left(\frac{V_{GS}}{nV_t}\right) \tag{7}$$

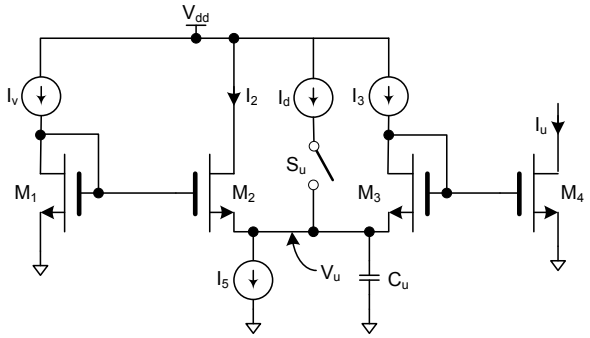


Figure 2. Accommodation variable (u) circuit

where I_0 is the drain current at $V_{GS} = 0$, W and L are the channel width and length, $V_t = kT/q$ is the thermal voltage (26mV at 300K), and $n = 1.2 - 1.4$. It can be shown [8] by utilizing the translinear principle and basic MOS subthreshold equations, that the relationship between the various currents for a four transistor log domain filter in Figure 2 is:

$$C n V_t \dot{I}_u = I_v I_3 - I_u (I_5 - I_3) \tag{8}$$

3.1. Accomodation Variable (u) Circuitry

By inspection, (3) is a first order low pass filter which can be directly implemented using the log domain filter building block with a modification for a reset term (I_d and S_u) as shown in Figure 2.

Comparing (6) and (8), simplifying for I_3 and I_5 and setting $a = 0.02$, $b = 0.2$, $nV_t \approx 0.03V$,

$$I_3 = 0.12 \times C\,[pF] \text{ and } I_5 = 6 I_3 \tag{9}$$

By choosing the operating speed of the circuit to be a factor of ten faster than real-time, we can minimize the area requirement for the design. We arbitrarily chose the capacitance to be $2\,pF$ which leads to $I_3 = 2.4pA$, $I_5 = 14.4pA$.

3.2. Membrane Voltage (v) Circuitry

The implementation of (2) is not as straightforward due to the presence of the positive feedback and non-linear terms. By adding in a positive feedback term using a current mirror consisting of M_4, M_6 and M_7, we can achieve the non-linear functionality in (2) as shown in Figure 3.

Applying the translinear principle for transistors M_1 through M_4 and KCL at node v and some algebraic manipulations to eliminate I_2 and V_v from the equations,

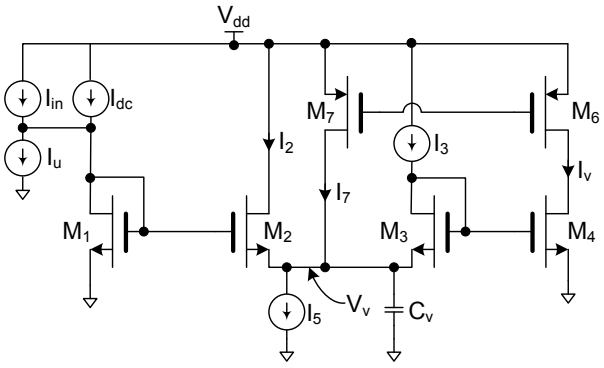


Figure 3. Membrane voltage (v) circuit

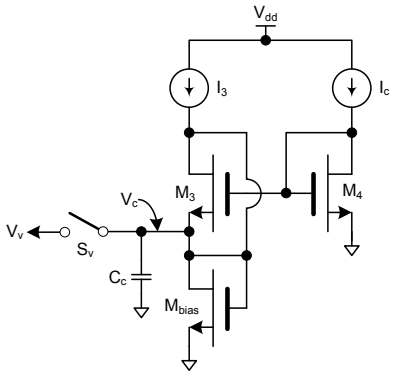


Figure 4. Membrane voltage (v) reset circuit

we get:

$$\frac{nV_tC_v}{I_3}\dot{I} = \frac{m}{I_3}I^2 - \left(\frac{I_5}{I_3} - 1\right)I + I_{dc} + I_{in} - I_u \qquad (10)$$

Where the positive feedback ratio $m = I_7/I_v$ can be set by the ratio of the sizes of transistors M_6 and M_7.

Comparing the above with (5),

$$a_2 = \frac{m}{I_3},\ a_1 = \left(\frac{I_5}{I_3} - 1\right),\ a_0 = I_{dc} \text{ where } \tau = \frac{nV_tC_v}{I_3} \qquad (11)$$

Substituting $b = 0.2$, we get $I_{dc} = 20pA$. For a design running ten times faster than real time, integer m and minimal currents, the smallest value of I_3 is $25pA$ for which $m = 1$, $I_5 = 4I_3 = 100pA$, $C_v = 0.0033I_3 = 0.083pF$.

3.3. Comparator and Reset Circuitry

The differential equations are by nature unstable once the membrane voltage exceeds a threshold. This condition results in a sudden increase in the membrane voltage similar to that experienced by the biological equivalent. The potassium influx is modeled by a reset term following the detection of a spike. The equations achieve this effect by forcing the membrane voltage to a reset value and also increment the accommodation variable.

The accommodation variable reset circuit shown in Figure 2 uses charge injection to add charge (proportional to the 'd' value) to the integrating capacitor. This simple circuit does not exactly reproduce the $u \leftarrow u + d$ as in the differential equation as the charge added/removed is now a function of the voltage across the capacitor. This effect is quite small however due to the current mode operation where node voltages do not change by large amounts during operation.

The membrane voltage is reset using a switch to a voltage source as shown in Figure 4. The reset value is determined by a circuit that mirrors the operation of the M_3 and M_4. Note that the reset is not instantaneous as in the differential equation. The behavior is similar to that of a real neuron where the spike has a finite rise and fall time. A small capacitor is used to improve the reset time.

4. Simulation Results

The design was simulated using the MOSIS $90nm$ library. Thick oxide devices were used for all transistors in this circuit to minimize gate leakage. The circuit consumes $0.2nW$ in the resting state and $7nW$ in the tonic spiking state. The core analog portion of this power (excluding the digital spike output interface) is a small fraction of this overall power, and corresponds to an energy of less than 1pJ for each spike, comparable to the energy consumed by action potential generation in biophysical neurons.

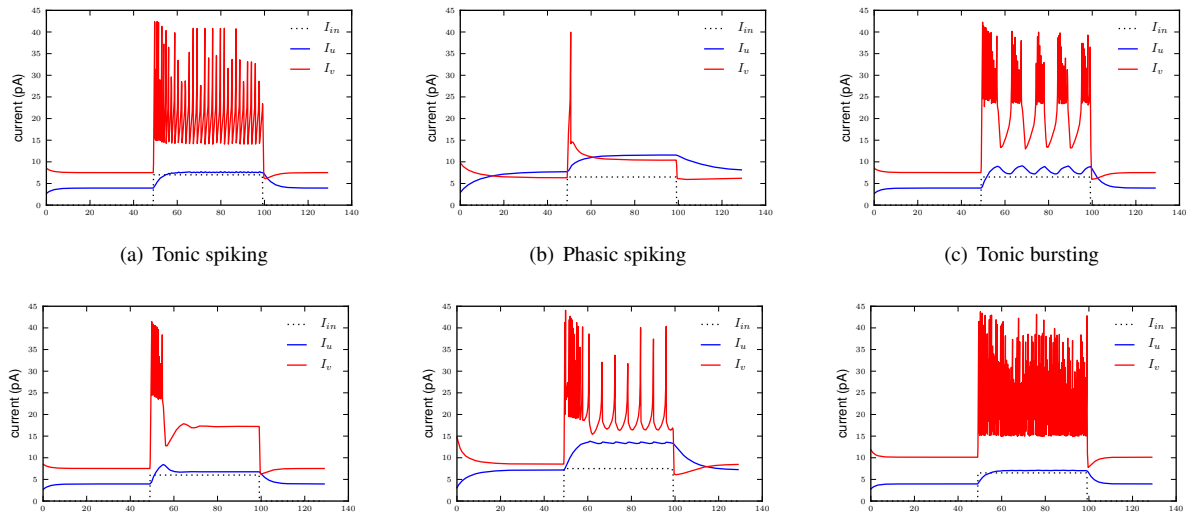
The circuit occupies an estimated $2980\mu m^2$ of which $2083\mu m^2$ is occupied by the integration capacitors for the u and v circuits.

Figure 4 shows the transient response to a step input current for various representative neuron types.

The circuit will be most sensitive to threshold voltage variations due to the exponential dependence of the current on gate voltage. It can be shown that the effect of mismatch in the four transistor translinear circuit causes a change in the slope in the u circuit. A mismatch in the v variable causes a change in the vertical position as well as the shape of the nullclines.

Based on [5], the above variations can be compensated for by either changing the slope of the u equation or by changing the offset of the v circuit to get back the original dynamics. This will necessitate some form of calibration if precise dynamics from each neuron are desired.

The effect of thermal noise has been investigated in



(a) Tonic spiking (b) Phasic spiking (c) Tonic bursting

(d) Phasic bursting (e) Intrinsic bursting (f) Fast spiking

Figure 5. The red trace is the Membrane voltage (I_v) for different spiking neuron behaviors while the blue trace is the accomodation variable (I_u) . The stimulus in all cases is a step input current, applied at 20 ms and removed at 80 ms as shown by the black trace. The x-axis for all plots is time in units of milli-seconds and the y axis is in units of pA after the transformation from (1).

simulations and the effect is to cause a jitter in the timing of the output spikes as compared to the case without noise.

5. Conclusion

We implemented the efficient two state variable representation described in the Izhikevich neuron model in a compact circuit architecture in analog VLSI.

The high efficiency of the compact neural model and its low-energy realization in analog VLSI make the architecture suitable for integration with dense synaptic arrays, such as [3], towards very large scale neuromorphic systems approaching the size and complexity of mammalian brain.

6. Acknowledgment

We would like to acknowledge the earlier work and discussions with Moon-Jung Kyung, Eric Weiss, Teddy Yu and Sidharth Joshi.

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