aVLSI Array of Spiking Neurons with Dynamical Synapses

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VLSI Neural Networks

• Challenge in representing synaptic connections between neurons on chip

• Address Event Representation
  • Use high speed digital bus to time multiplex spike events
  • Neurons in an array (like RAM or image data)
  • Dynamic connections between neurons on array
I&F Neuron Model

- Must be compact
- Membrane potential as voltage on capacitor
- Synapse as a current source charging membrane capacitor
- Spike generator when membrane voltage reaches threshold
- External reset after spike
VLSI Synapses

• Current Source
• Switched Capacitor Conductance
• Integrator
• Floating Gate
• Full Biophysical Model
Neuron Design

• Integrate and Fire Neuron (Goldberg 2001) with AER interfacing
• Positive feedback loop to generate spike events
• Programmable threshold
Synapse Design

- Inspired by Batolozzi and Indiveri, 2007
  - Simplified and “enhanced”
- Two stages
  - Spike Filter and Current Pulse Generator
  - Conductance between synaptic reversal potential and membrane voltage
Synapse-Neuron Pair

- Connected a single excitatory synapse to I&F Neuron
- Tested synapse-neuron response for different spike input frequencies