Week 1

VLSI Technology and Device Characterization

References

2. Tsividis, Operation and Modeling of the MOS Transistor.
3. Sze, VLSI Technology.
SILICON VLSI TECHNOLOGY

INGREDIENTS
- Silicon
- Polysilicon (POLY)
- Oxide (SiO₂)
- Impurities (diffusion, implants)
- Metal (Al, Au)

DEVICES
- MOSFETS (nMOS, pMOS)
- JFETS
- Bipolar (nnp, pnp)
- Diodes
- Capacitors
- Resistors
  + derivatives: phototransistors, floating gates, CCD's, ...

LAYERS (typical MOSIS)
- Diffusion (n and p; masked with "Select")
- Well
- Poly (poly1, poly2)
- Metal (metal 1, metal 2, ...)
- p-base (nnp vertical BJT in n-well process)
- Buried channel
+ Contacts; Via(s)
MOS TRANSISTORS

(a) top view

(b) $V_{GS} = 0$, $V_{DS} = 0$ (cutoff)

(c) $0 < V_{GS} < V_T$, $V_{DS} = 0$ (cutoff)

(d) $V_{GS} > V_T$, $V_{DS} = 0$ (ohmic)

(e) $V_{GS} > V_T$, $V_{DS}$ small pos. (ohmic)

(f) $V_{GS} > V_T$, $V_{DS}$ large pos. (saturated)

FIGURE 2.2.3
Typical output characteristics for an n-channel MOSFET.
MOS MODELS

Above threshold: (Shichman-Hodges)

\[ I_D = \begin{cases} \frac{1}{2} k' \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) & \text{CUTOFF} \\ k' \frac{W}{L} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS} (1 + \lambda V_{DS}) & \text{SATURATION} \\ V_T = V_{TO} + \gamma (\sqrt{\phi - V_{BS}} - \sqrt{\phi}) & \text{OHMIC (TRIODE)} \end{cases} \]

Below threshold:

\[ I_D = I_0 \cdot \frac{W}{L} \cdot e^{\frac{kV_{GB} - V_{SB}}{V_{th}}} \left(1 - e^{-\frac{V_{DS}}{V_{th}}}\right) (1 + \lambda V_{DS}) \]

\[ V_{th} = \text{thermal voltage, } \frac{kT}{q} \approx 25 \text{ mV} \]

\[ k = \text{back gate effect} \]

AC, small signal:

![Diagram of MOS device](image)

FIGURE 3.1.19
MOS symbols:

- n-channel enhancement
- p-channel enhancement
- n-channel depletion
- p-channel depletion
- alternate n-channel notation
- alternate p-channel notation
- simplified enhancement
- simplified depletion
- simplified n-channel
- simplified p-channel
- electric variable convention
  (n- or p-channel, enhancement or depletion)

FIGURE 2.2-4
Symbols for MOS transistors.
PHYSICAL LAYOUT / PARASITICS:

CIF:

Cross section:

FIGURE 2.2-7
Parasitic transistors in a p-well CMOS process.
BIPOLAR JUNCTION TRANSISTORS (BJT's)

<table>
<thead>
<tr>
<th>Pictorial Description</th>
<th>Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>npn</strong></td>
<td></td>
</tr>
<tr>
<td>n-type</td>
<td>Collector</td>
</tr>
<tr>
<td>p-type</td>
<td>Base</td>
</tr>
<tr>
<td>n-type</td>
<td>Emitter</td>
</tr>
<tr>
<td><strong>pnp</strong></td>
<td></td>
</tr>
<tr>
<td>p-type</td>
<td>C</td>
</tr>
<tr>
<td>n-type</td>
<td>B</td>
</tr>
<tr>
<td>p-type</td>
<td>E</td>
</tr>
</tbody>
</table>

**DC:**

\[
I_C = J_s A e^{V_{BE}/V_t} \left( 1 + V_{CE}/V_{AF} \right)
\]

\[
I_B = \frac{1}{\beta_f} J_s A e^{V_{BE}/V_t}
\]

**AC:**

---

**FIGURE 2.2-8**
Bipolar transistors.

**FIGURE 3.3-12**
High-frequency small signal equivalent circuit of BJT.
Bipolar process (w/ epi layers)

Through MOSIS (BiCMOS):

- Vertical:

- Lateral:

(almost useless as BJT)
NOTE: SCR (thyristor; npnp or pnpn)

\[ I = I_{E_2} \]

\[ I_{C_1} = \beta_1 I_{B_1} = \beta_1 (I_{C_2} + C_{p_2} \frac{d}{dt} V_{p_2}) \]

\[ I_{C_2} = \beta_2 I_{B_2} = \beta_2 (I_{C_1} - C_{p_2} \frac{d}{dt} V_{p_2}) \]

\[ \beta_1, \beta_2 \gg 1 \Rightarrow \frac{I_{C_1}}{I_{B_1}^2} \rightarrow \infty \Rightarrow O \]

BIStABLE
# Comparison

<table>
<thead>
<tr>
<th>MOS</th>
<th>Bipolar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage-driven current source</td>
<td>Current-driven current source</td>
</tr>
<tr>
<td>$Z_{in} = \infty$</td>
<td>$Z_{in} = \text{small}$</td>
</tr>
<tr>
<td>$Z_{out} = \text{large}$</td>
<td>$Z_{out} = \text{large}$</td>
</tr>
<tr>
<td>Ohmic insulation</td>
<td>Low-noise</td>
</tr>
<tr>
<td>Compact</td>
<td>Precise matching</td>
</tr>
<tr>
<td>Thermally stable</td>
<td>Fast</td>
</tr>
</tbody>
</table>
| Logic / memory (no static power) | High-speed interfacing (ECL, ...)
| Switched capacitors | Linear analog |

**BiCMOS VLSI**
Slow recovery of inversion channel, unless there are drain and source diffusions in contact with the channel to provide carriers fast.
CCD's (and CID's)
Basic CCD Shift Register Operation

Fig. 1.7 (a)–(e) Movement of potential well and associated charge packet by clocking of electrode voltages; (f) clocking waveforms for a three-phase CCD.
Buried Channel CCD

To reduce effects of interface traps by pushing the carriers further below the oxide

Input Diode

$+20V$

SiO$_2$

Transfer Electrodes

$+15V$

$0V$

n-Si

p-Si

Output Diode

$+20V$

n$^+$

--- Equipotential Lines

--- Transfer Channel

Same as surface channel CCD except for a weak n implant underneath the CCD gates.
Fig. 2.12 Capacitor equivalent circuits for (a) surface-channel and (b) buried-channel CCDs.

**SURFACE CHANNEL**

*PRO:* STANDARD CMOS TECH.
- LINEAR \( Q(V) \)

*CON:* INTERFACE TRAPS

**BURIED CHANNEL**

*PRO:* BETTER CHARGE TRANSFER EFF.

*CON:* HIGHER VOLTAGES TO DRIVE
- NONLINEAR \( Q(V) \)
- EXTRA PROCESSING LAYER
OTHER DEVICES:

- JFET:

- Phototransistors, photodiodes: Same as BJT s, diodes (base of the phototransistor needs to be left floating to collect photocurrent)

- Linear capacitors:

- Linear resistors: poly strings ($\text{SHEET} \approx 20 \Omega/\square$)

  Hi-RES: 1000 $\Omega/\square$

  (0.5um AMIS)